Greetings from Olaf Vogt

Director and Head of Application Marketing

Olaf Vogt
Director and Head of Application Marketing

"I would like to thank all participants for joining this first-of-its-kind Nexperia virtual ESD seminar.

*The **automotive industry** is driven by the major trends of **electrification, autonomous driving and shared 'connected' mobility**.*

*We also see that ever-increasing data rates, greater calculation power of System-on-Chips and IC miniaturization are making **systems even more sensitive to ESD**.*

*With our Nexperia ESD Seminar, we want to **support the design community** in protecting applications and products against ESD issues and make systems more reliable.*

*Additionally, we published an **automotive ESD application handbook to share our expertise and best practices with you."***

ESD
APPLICATION HANDBOOK
AUTOMOTIVE EDITION
PROTECTION CONCEPTS, TESTING & SIMULATION FOR MODERN INTERFACES
Design Engineer's Guide
nexperia

nexperia

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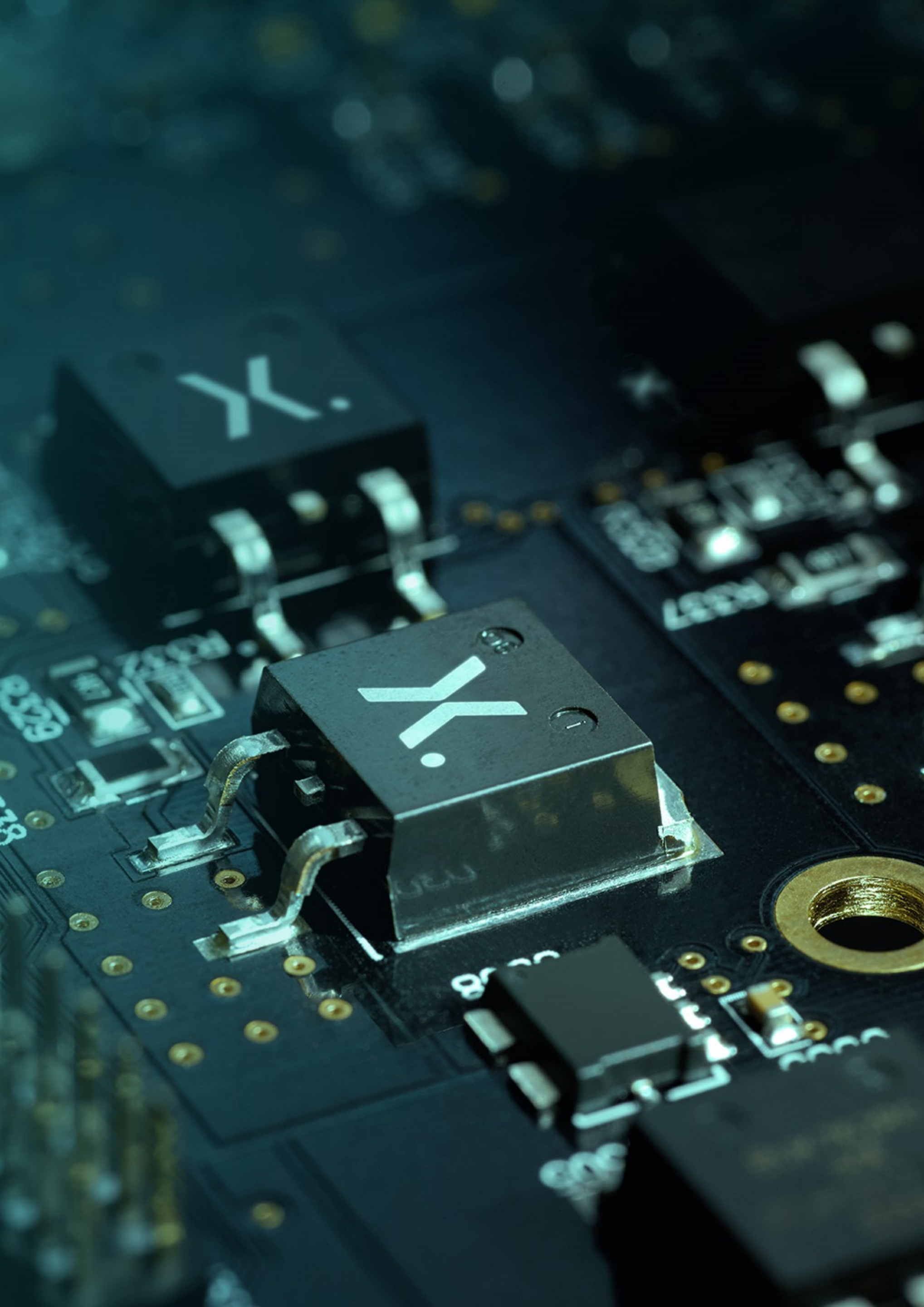
Sept. 2020



ESD Seminar Session 1

Agenda

- **Fundamentals of ESD Protection**
- Measurement and Characterization
- Nexperia Lab
- Q&A

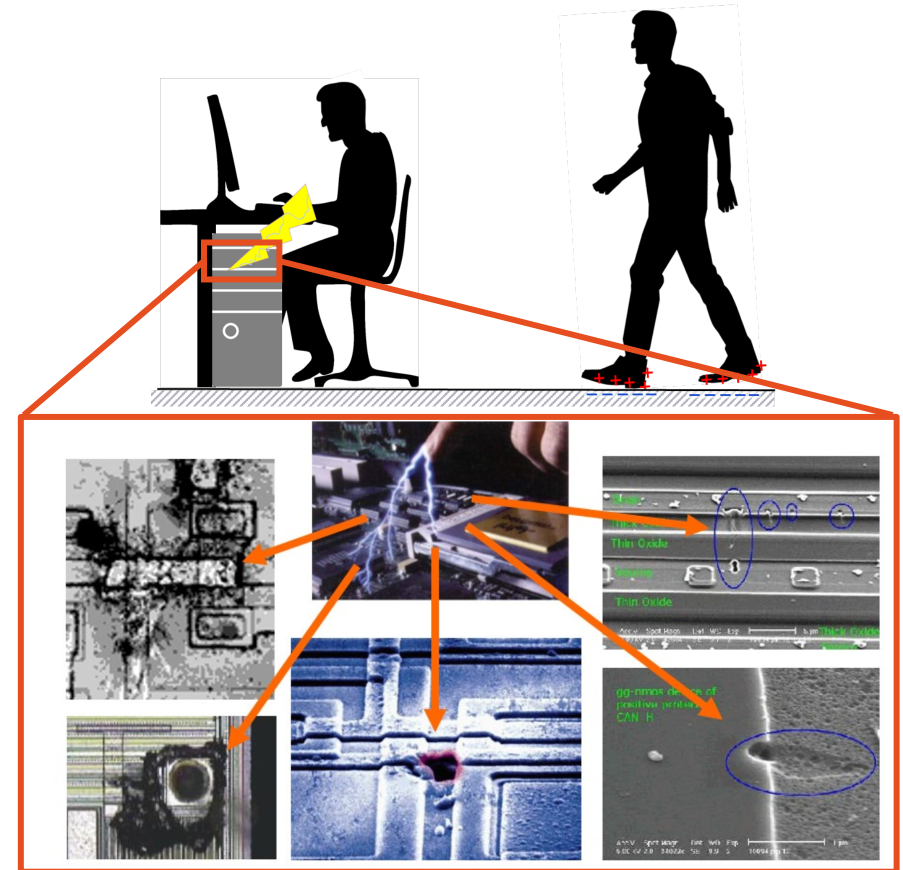
ESD – Electro Static Discharge

WHAT

A sudden discharge between persons, devices or components

HOW

- A charged person touches an integrated circuit (IC)
- A charged IC drops on a grounded metal plate
- A charged machine touches an IC
- An electrostatic field is induced by high voltages

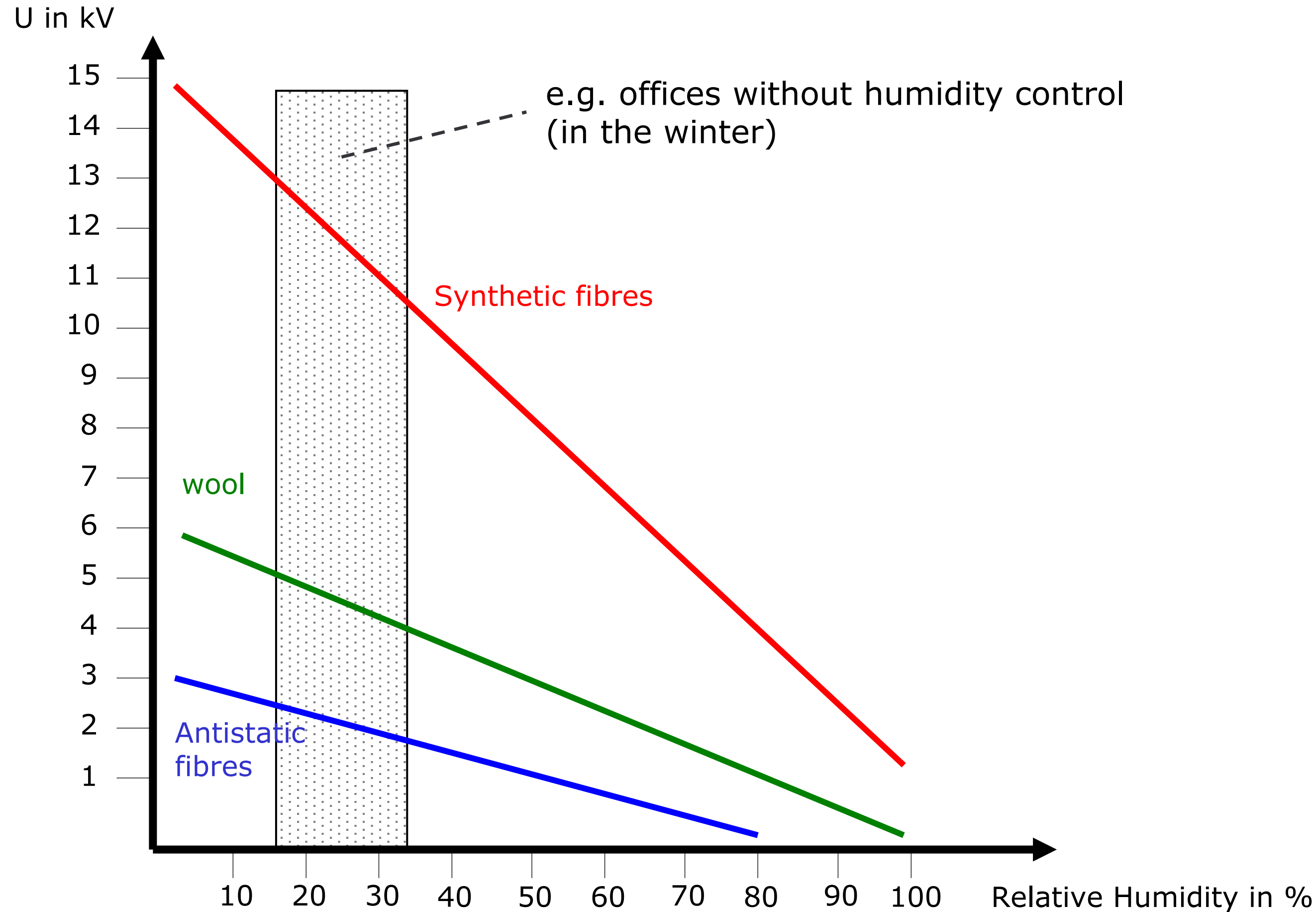


PROBLEM

- Causing malfunction (reversible by power-off-on cycle)
- Destruction of electrical components (irreversible): gate oxide, metallisation or PN junctions

ESD – Electro Static Discharge

Material / environmental influences affect charge separation

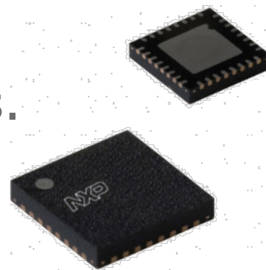


Many materials have potential to cause ESD events

ESD – Electro Static Discharge

Device level

- ICs can be destroyed (ESD) during placement.
- ESD "on-chip protection" protects against defects during production.
- Qualification by standards (JEDEC)
  - Human Body Model (HBM)
  - Machine Model (MM)
  - Charged Device Model (CDM)
- ESD pulses are given to all IC pins.



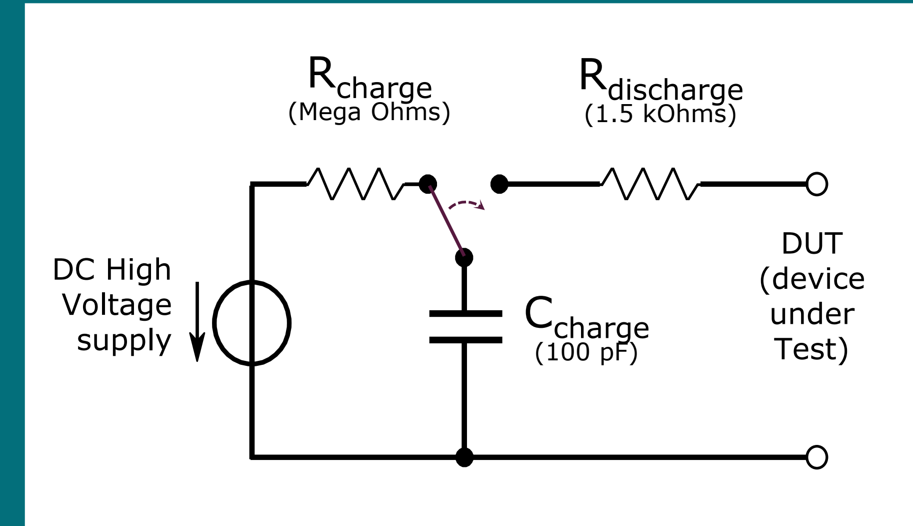
System level

- ESD threatens also boards and (complete) devices.
- Special diodes are added on the board to avoid destruction by ESD.
- "System Level" ESD standards
  - IEC 61000-4-2
    Electrostatic discharge immunity test
  - ISO 10605
- ESD pulses are given to certain accessible interfaces.
  Individual components are not tested!

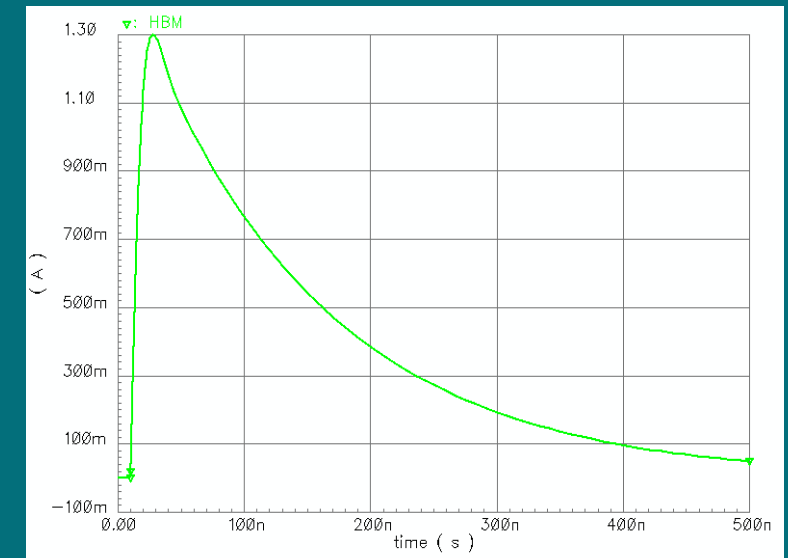
ESD – Device Level Testing: HBM

Human Body Model

- HBM was developed to simulate the discharge of a human body to a grounded device (IC).
- To replicate an RC network is used:
  - R = 1500 ohms
  - C = 100 pF
- ANSI / ESDA / JEDEC JS-001-2012 for Semiconductor Components
- **Different** from standard EN 61000-4-2 for devices (system level test)



Low current – long duration

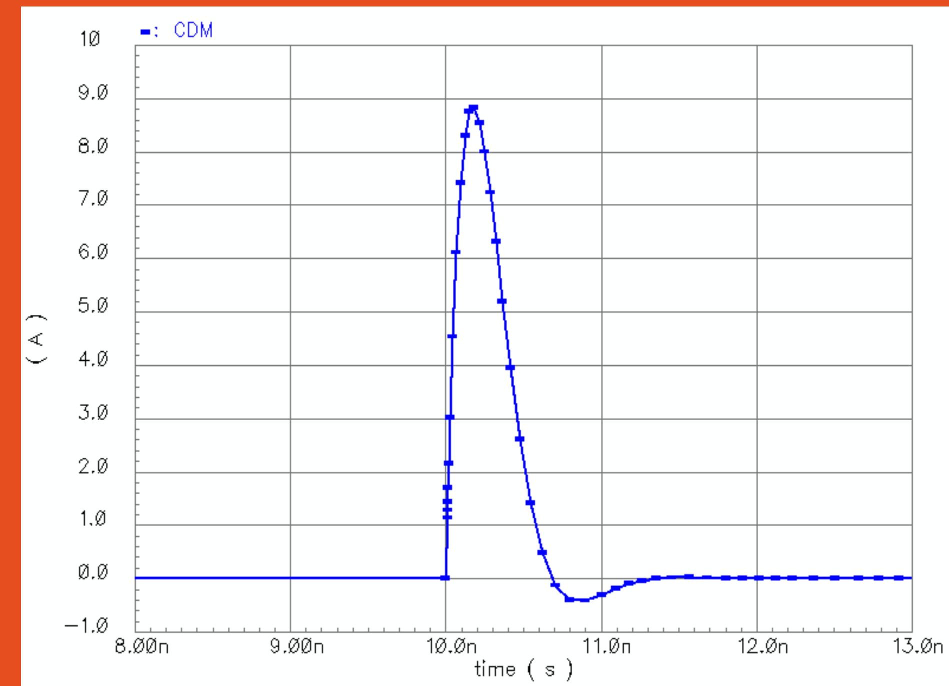


ESD – Device Level Testing: CDM

Charged Device Model

- CDM emulates the process of charging / discharging that can occur in production environments.
- For example, ICs that are poured from plastic tubes and hit a metallic surface.
- It is conceivable that charges have accumulated on the metal pins of an IC or on the package, ultimately discharging through a single grounded pin.
- The discharge current is limited only by parasitic impedances and capacitance.

Very high current –
very short pulse duration



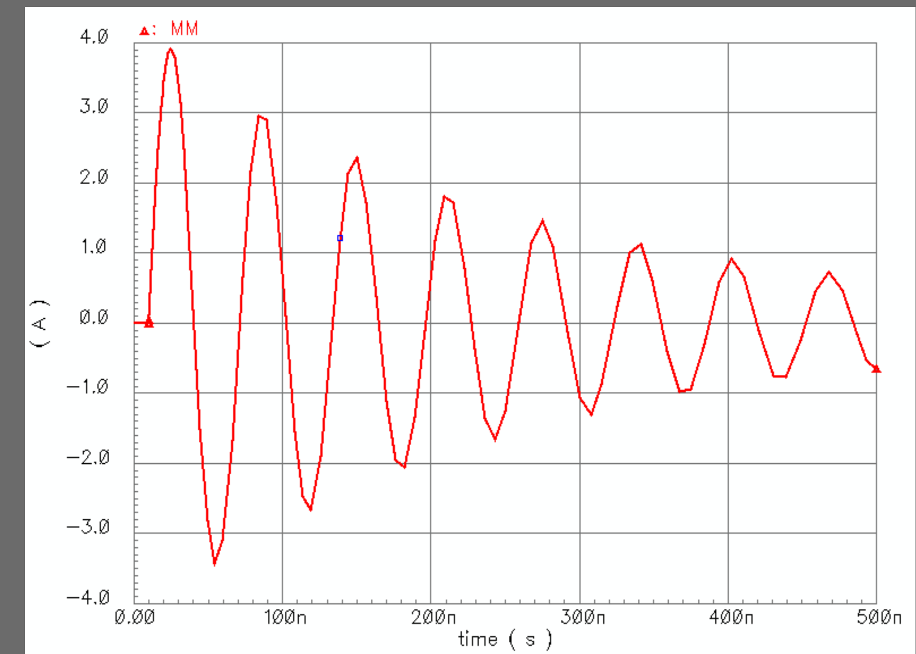
ESD – Device Level Testing: MM

Machine Model

- MM was developed to model the discharge of a machine to a grounded device (IC).
- Here an RC network is used:
  - R = <1 ohm
  - C = 200 pF
- Usually replaced by HBM and CDM:
  „… JEDEC has strongly recommended discontinuing use of the MM for ESD qualification because of its test variability and non-correlation to real world failure modes"

  https://www.esda.org/assets/Uploads/documents/The-Machine-Model2012.pdf

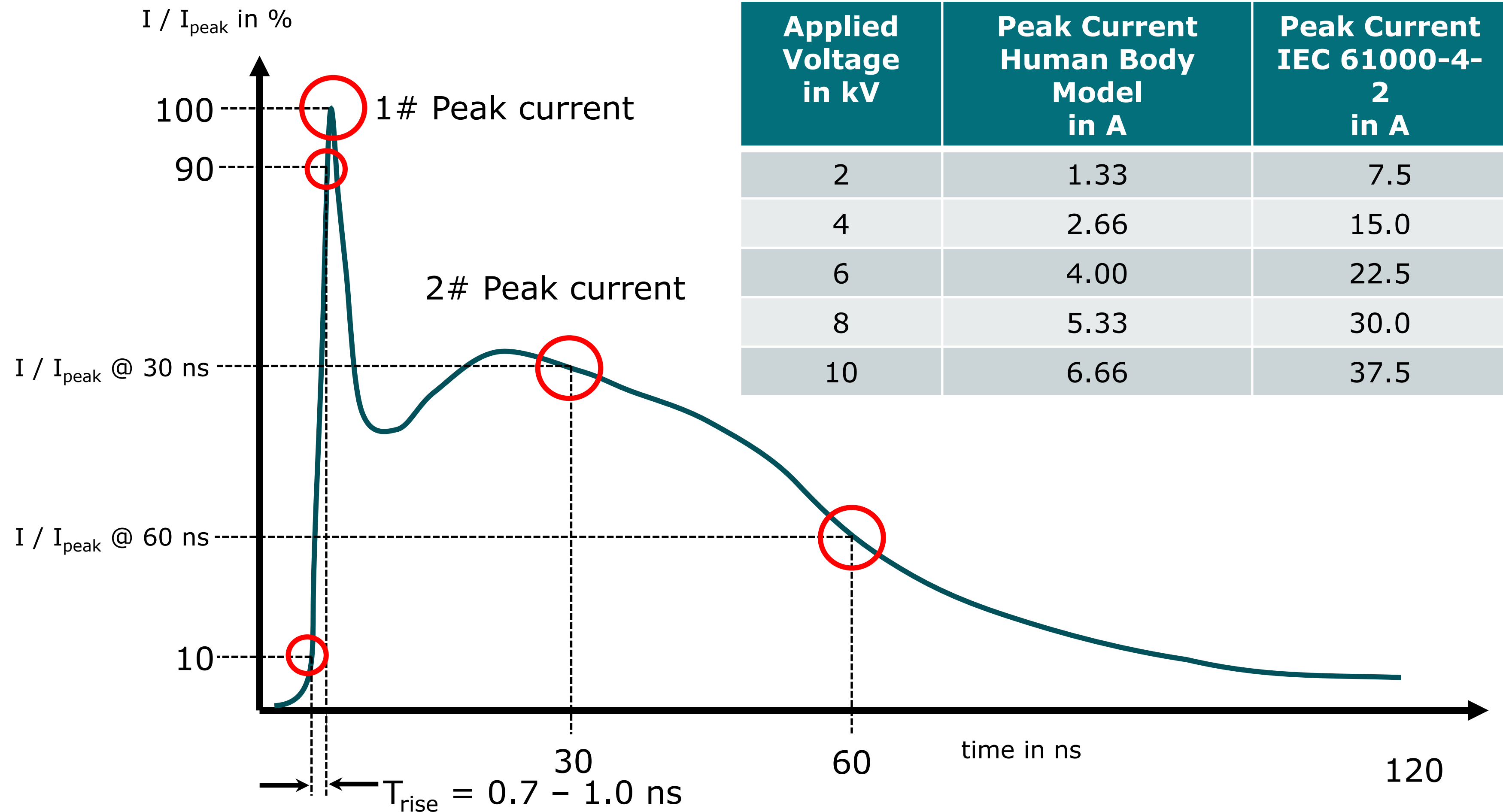
High current – long duration



ESD – System Level Testing: IEC 61000-4-2

Typical waveform of ESD current

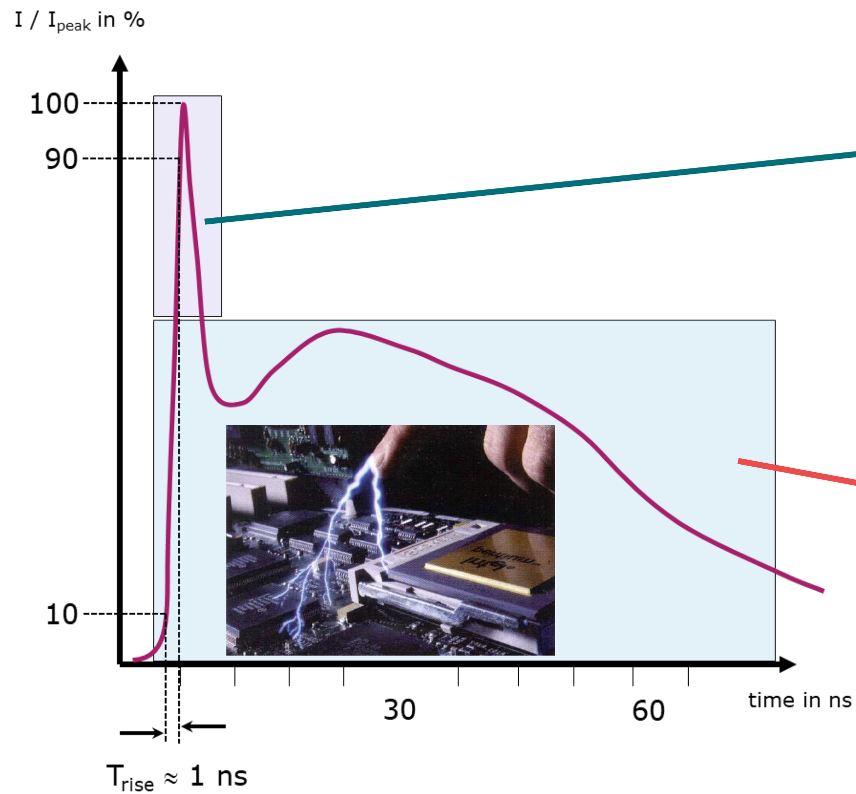
- Rise time
  - 0.7 – 1 ns
    (von 10% auf 90%)
- Peak current
  - +/- 10% tolerance
- Current after 30 ns
  - +/- 30% tolerance
- Current after 60 ns
  - +/- 30% tolerance



Applied Voltage in kV	Peak Current Human Body Model in A	Peak Current IEC 61000-4-2 in A
2	1.33	7.5
4	2.66	15.0
6	4.00	22.5
8	5.33	30.0
10	6.66	37.5

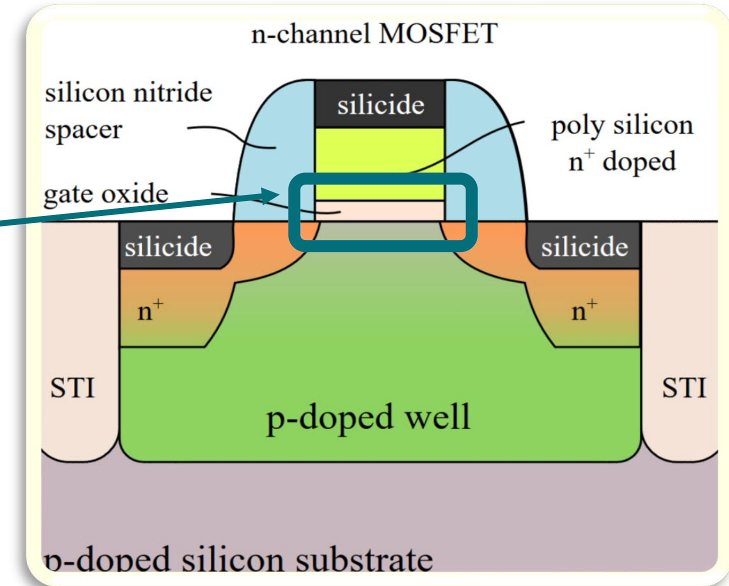
ESD – Defects caused by ESD

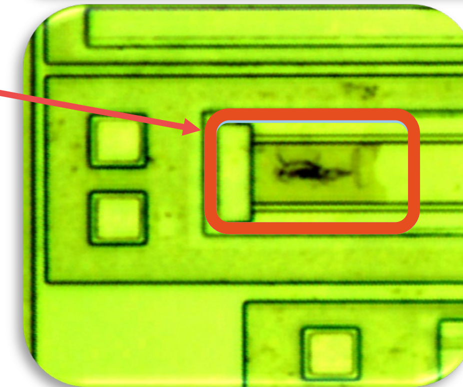
Destruction mechanism



High voltage

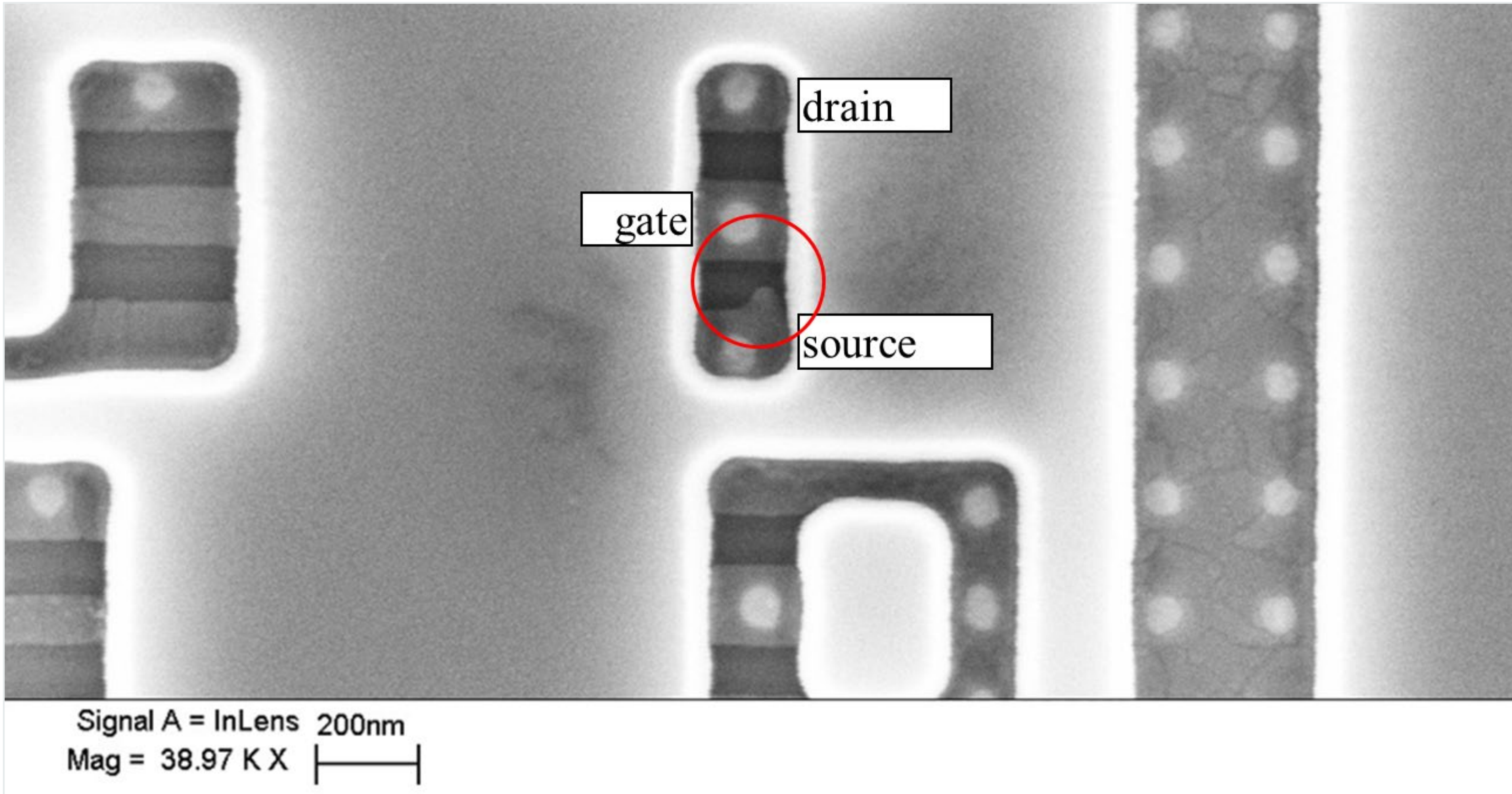
High energy





ESD – Defects caused by ESD

Destruction mechanism

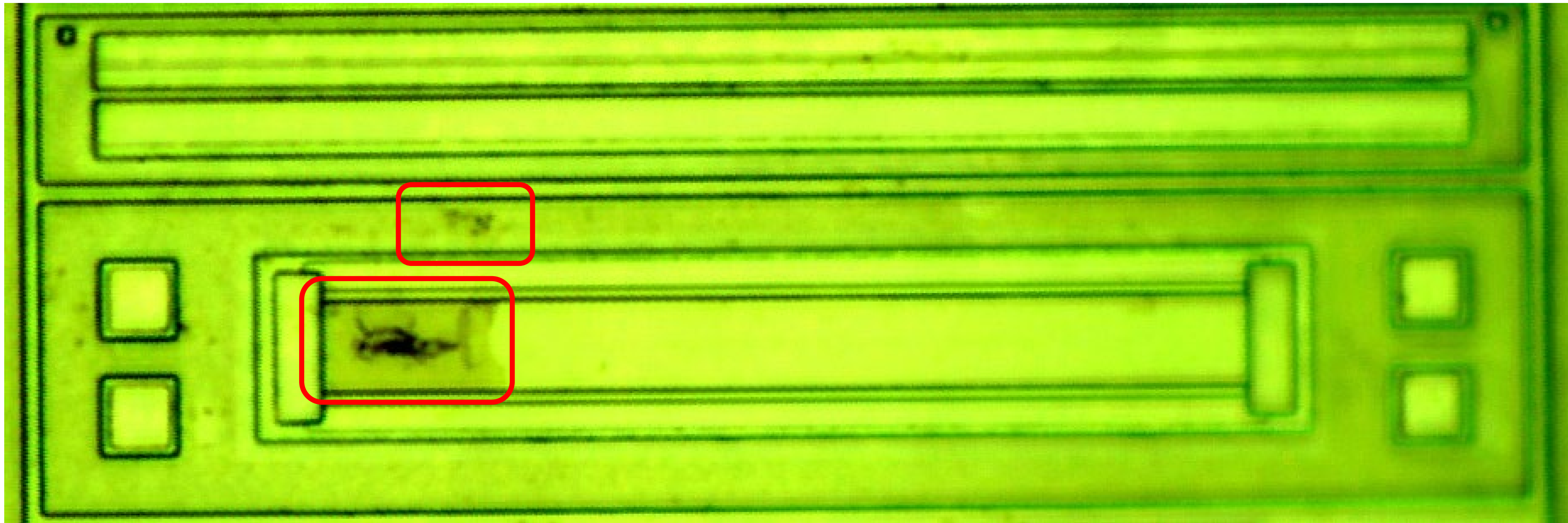


Bottom (!) view of gate oxide damage after CDM discharge

Deprocessing consisted of grinding Si backside until 4µm and removing the remaining Si using a highly selective etch which stops at the SiO2.

ESD – Defects caused by ESD

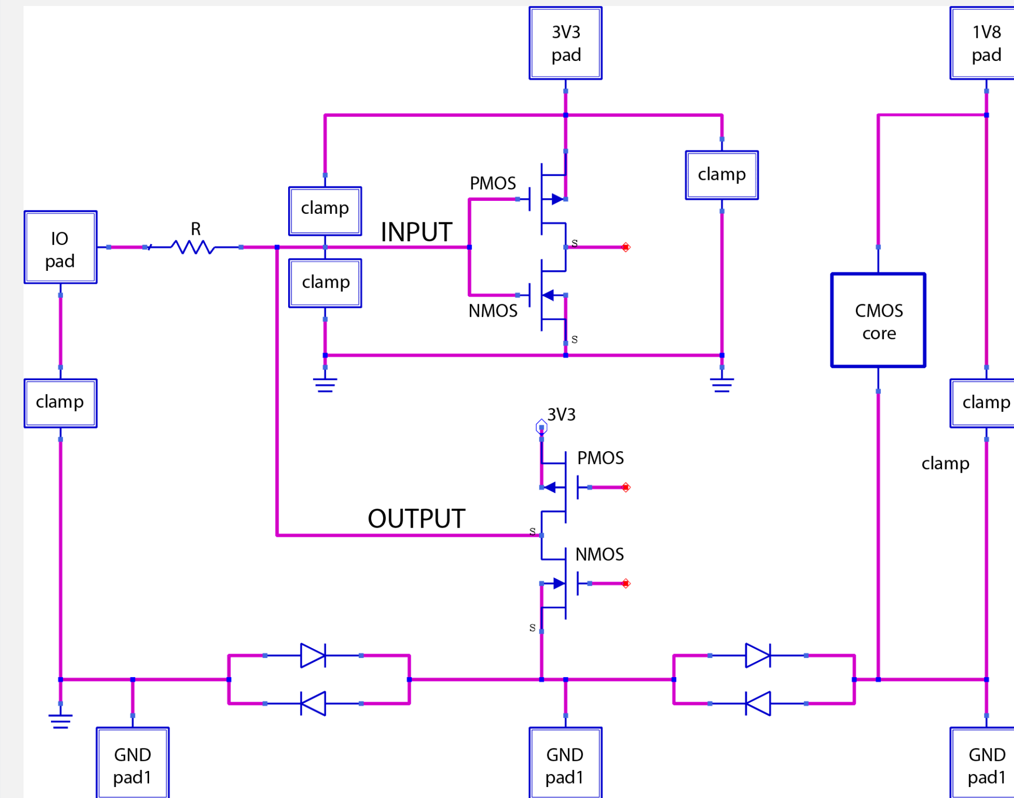
Destruction mechanism



Microscope picture of melt damage in large transistor

ESD – Protection Strategies inside ICs

- Integrated circuits (ICs) are usually protected by internal measures against ESD damage.
- **This protection is usually only sufficient for manufacturing processes!**
- Devices with external interfaces (e.g., CAN, 100Base-T1, USB, HDMI, ...) usually require additional external ESD protection!



ESD – Protection Strategies inside ICs

PMZB670UPE

20 V, single P-channel Trench MOSFET

Rev. 3 — 23 March 2012 **Product data sheet**

1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1006B-3 (SOT883B) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Very fast switching
- Low threshold voltage
- Trench MOSFET technology
- ESD protection up to 2 kV
- Ultra thin package profile of 0.37 mm

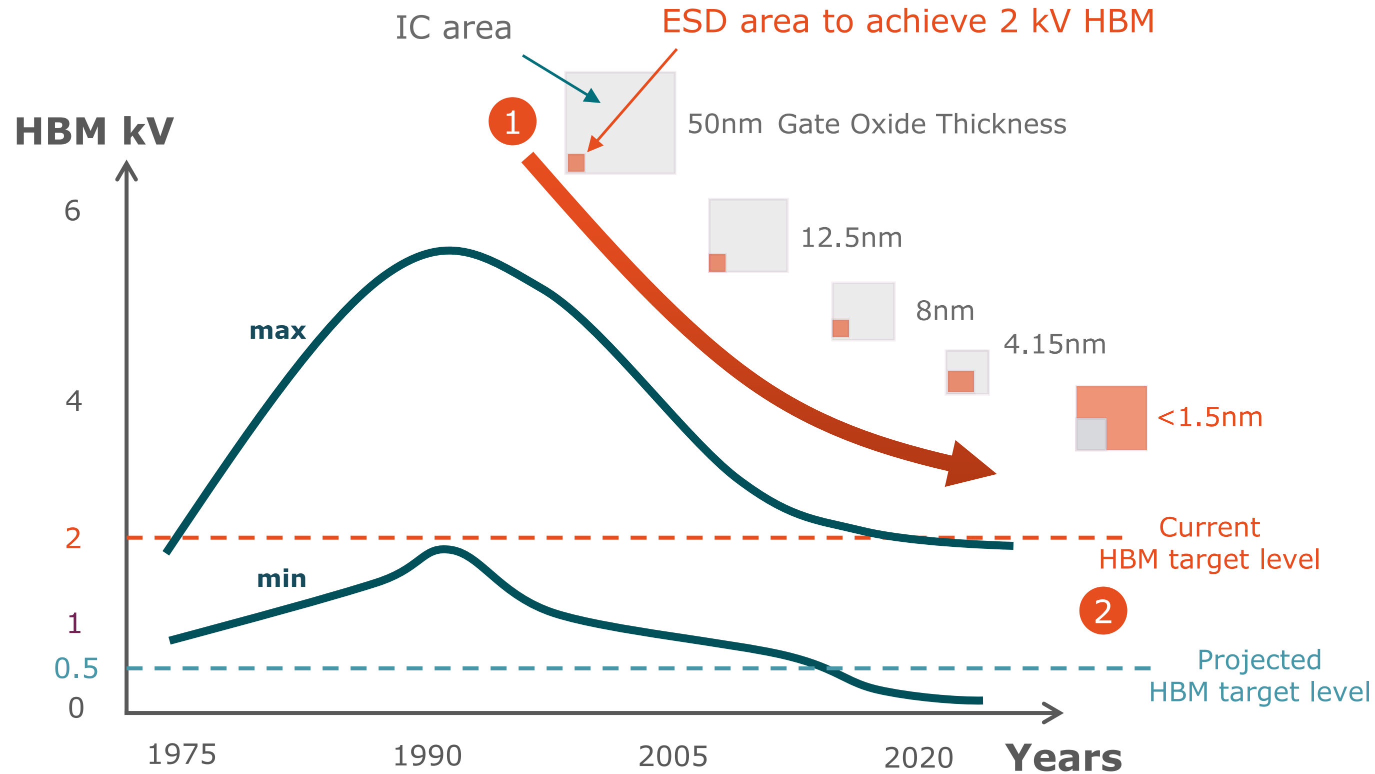
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source		
3	D	drain		

ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V

[3] Measured between all pins.

ICs become more sensitive

Increased performance and density lower the SoC ESD robustness



1 **ICs becoming more sensitive**

- Gate thickness and chip size (channel length) decreases
- Maximum gate voltage decreases (e.g. for CMOS090 <1.5V static)
- New Processes are optimized for area and performance

2 **HBM targets will be lowered**

- HBM targets will be lowered to meet device level ESD robustness
- HBM target already lowered down to 1 kV
- This trend is applicable for **CDM targets**

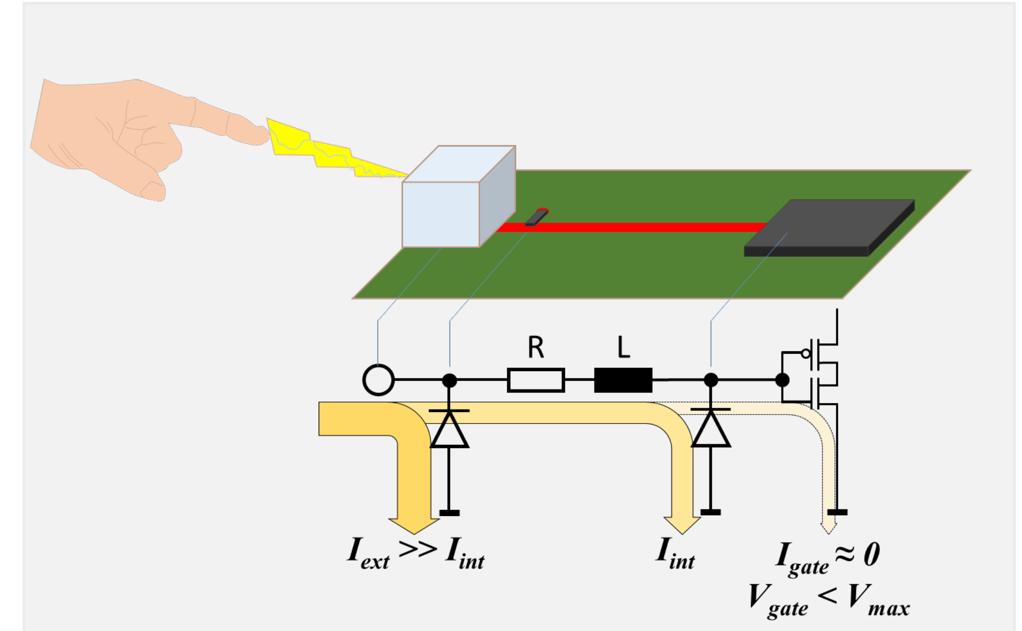
Source:
ESDA, 2016
Duvvy/Miller, 2009

IC robustness will decrease and require more dedicated discrete ESD solutions

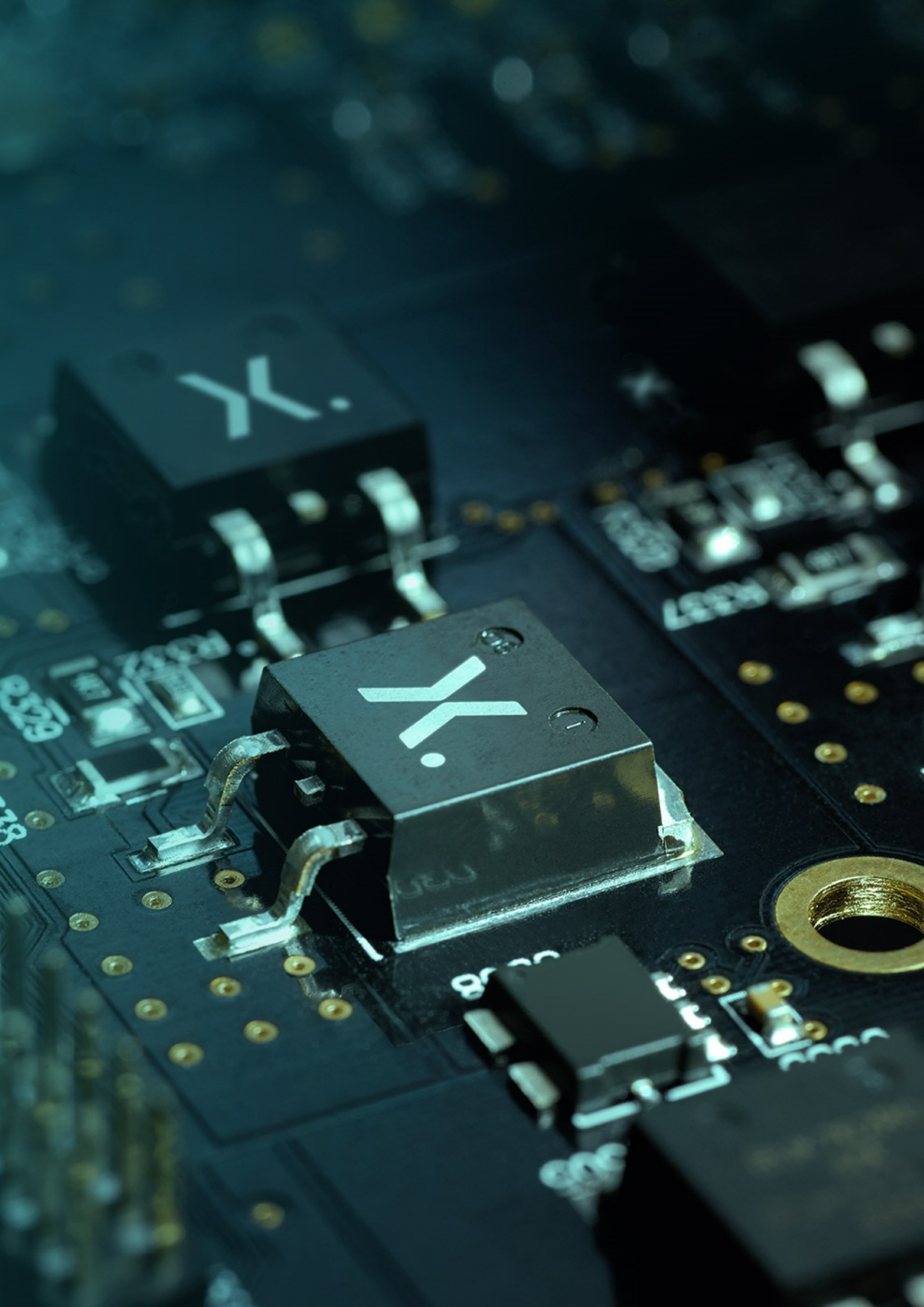
Benefits of external ESD protection

Example CAN bus with PESD2IVN24-T

IC/Transceiver	ESD robustness w/o	ESD robustness with PESD2IVN24-T
TLE 9263BQXV33XUMA1	+ 8 kV (HBM)	+ 30 kV
TLE 9262BQXXUMA1	+ 8 kV (HBM)	+ 30 kV
MCP25625 E/SS	+ 8 kV (HBM)	+ 30 kV
LPC11C22FBD48/301	+ 8 kV (HBM)	+ 30 kV
SN65HVD232QDRQ1	+ 11 kV (HBM)	+ 30 kV
TLE7250GXUMA1	+ 10 kV (HBM)	+ 30 kV
TJA1042T/3,118	+ 12 kV (HBM)	+ 30 kV
TJA1044T	+ 10 kV (HBM)	+ 30 kV
⋮	⋮	+30 kV



External ESD Protection can handle much **more current** and can be chosen **application specific**.



ESD Seminar Session 1

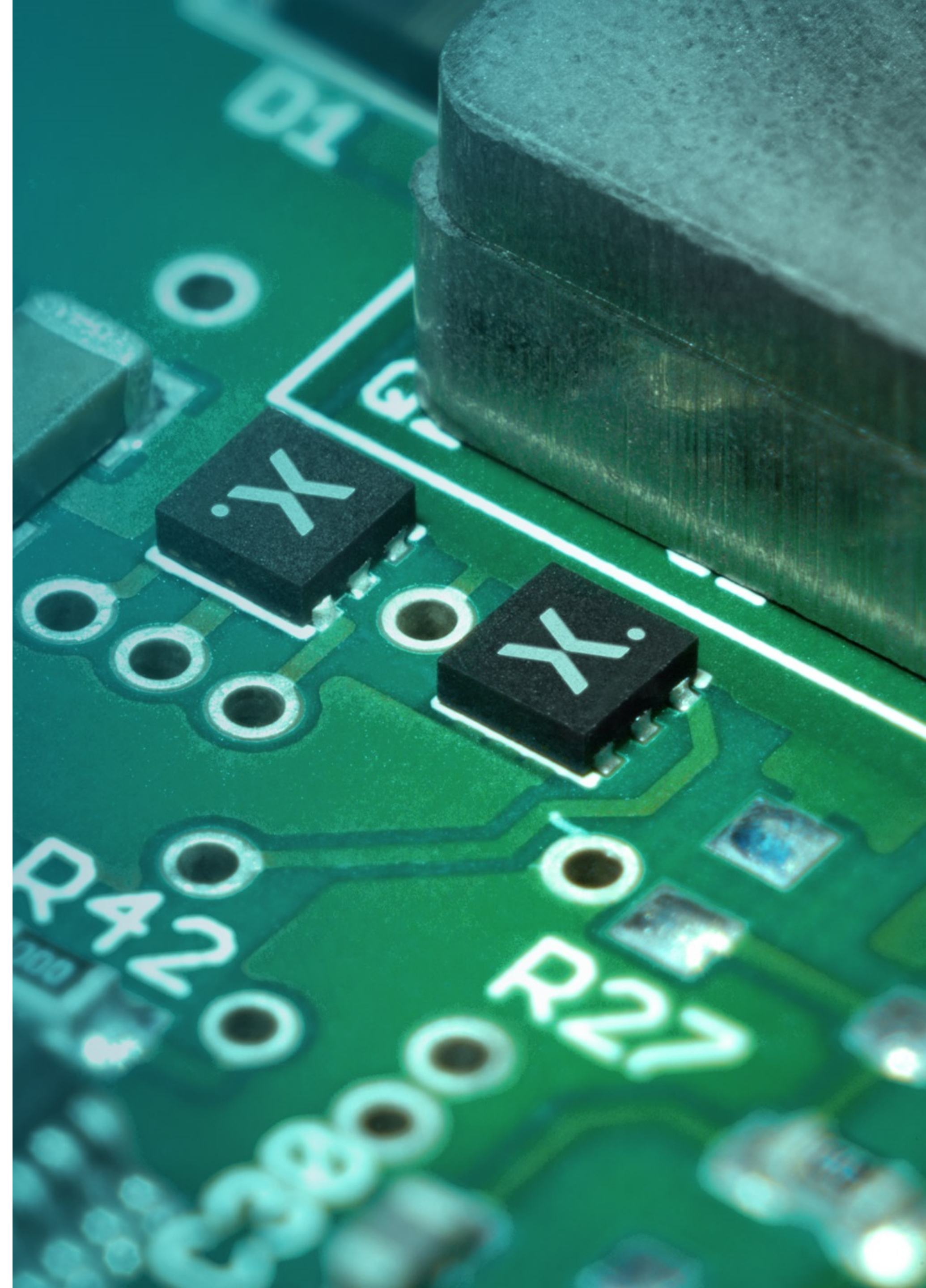
Agenda

- Fundamentals of ESD Protection
- **Measurement and Characterization**
- Nexperia Lab
- Q&A

Measurement and Characterization

Agenda

- Selection Criterion
- ESD Tolerance Test
- Clamping Voltage
- Peak Pulse Current
- Dynamic Resistance using TLP

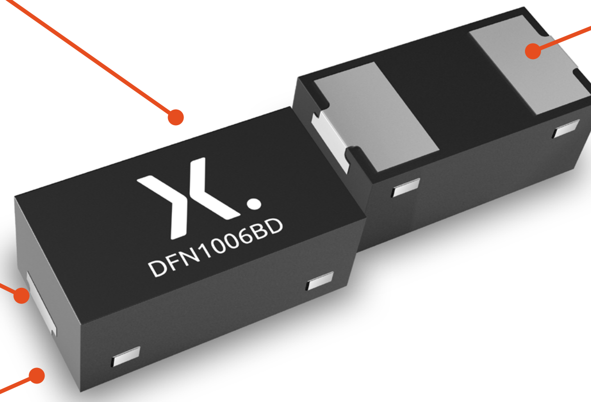


Selection Criterion

Package (shape/size/footprint)

Side-wettable flanks for AOI

Number of signal lines



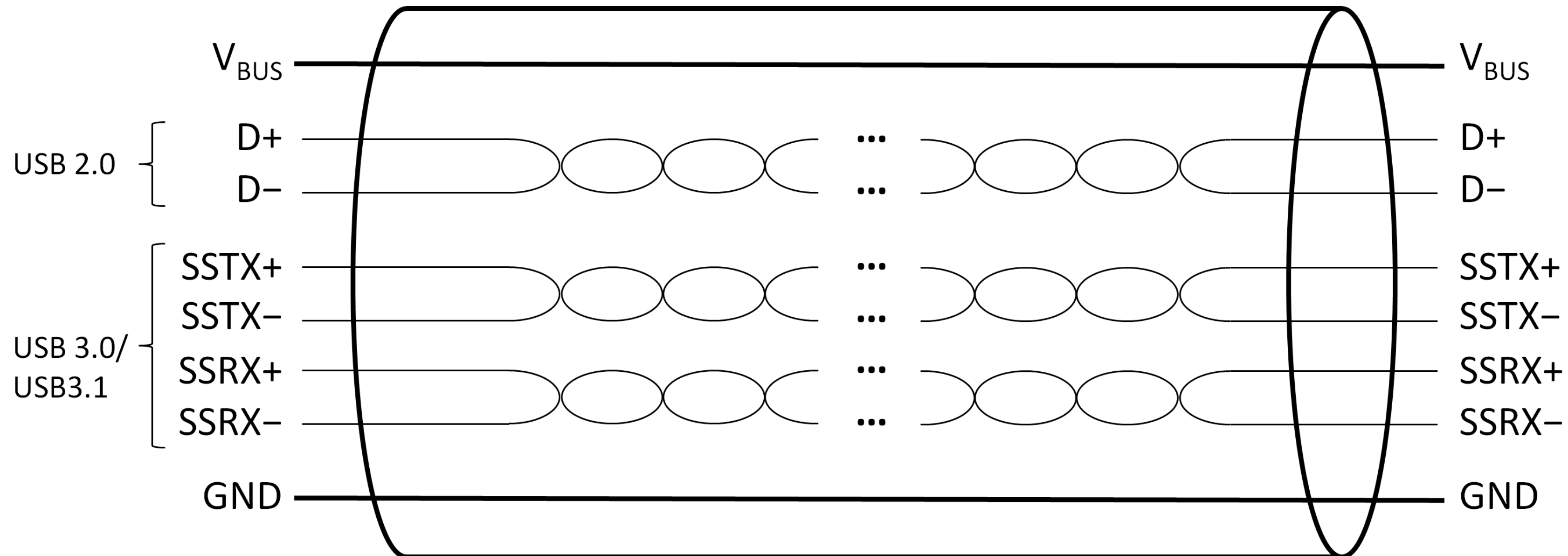
Electrical performance

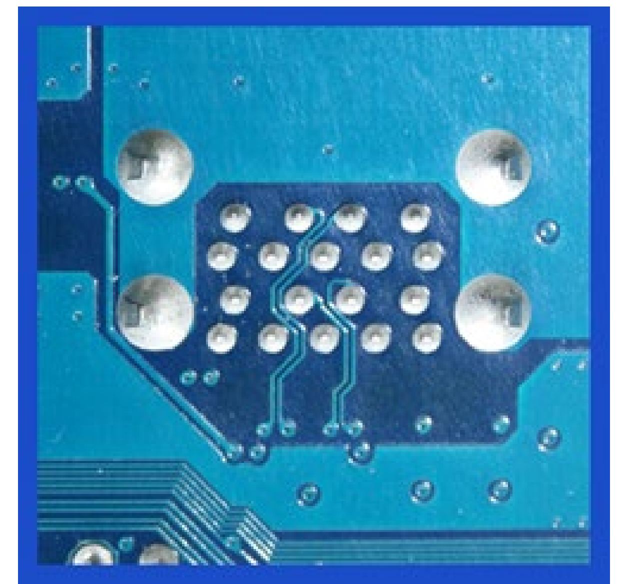
- Reverse stand-off voltage V_{RWM}
- ESD robustness level V_{ESD}
- Clamping voltage V_{clamp}
- Dynamic resistance R_{dyn}
- Topology: uni- / bi-directional, rail to rail, …
- Device capacitance C_{diode} and other parasitics

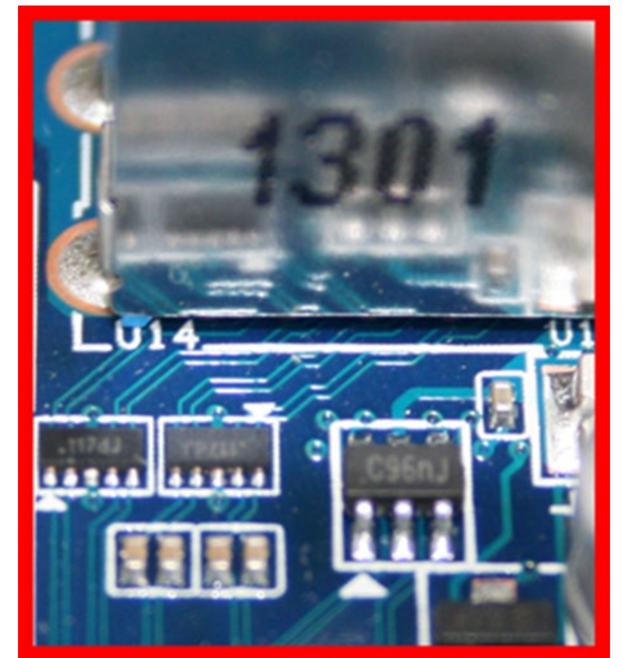
Selection Criterion

Selection Criteria: Number of signal lines

- Single signal line vs. multiple similar lines, e.g. USB 3.0





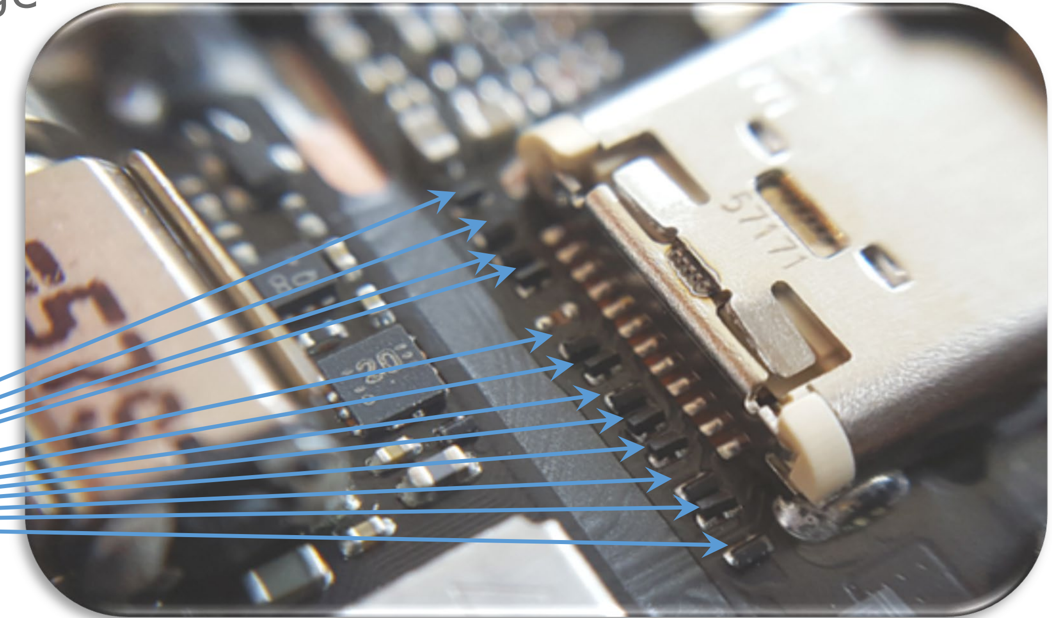


Selection Criterion

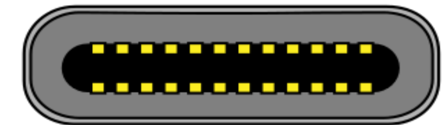
Selection Criteria: Number of signal lines / Package

- Number of „pick and place“ cycles
- Stock keeping
- Bulk purchase
- Second source
- Easy routing (layout)

By courtesy of ASM Assembly Systems



By courtesy of M. Pilaski



commons.wikimedia.org

Type-C

Selection Criterion

Reverse Working Maximum Voltage V_{RWM}

- PESD2IVN24-T

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	T_{amb} = 25 °C		-	-	24	V
V_{BR}	breakdown voltage	I_R = 10 mA; T_{amb} = 25 °C	[1]	25.5	30.5	35.5	V
I_{RM}	reverse leakage current	V_{RWM} = 24 V; T_{amb} = 25 °C	[1]	-	1	50	nA

ESD Tolerance Test – Measurement Equipment

ESD Simulator (Gun):

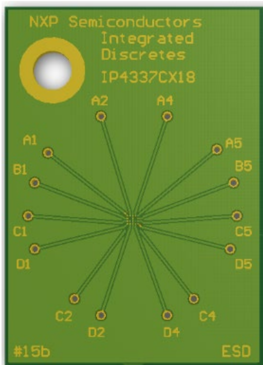
ESD 30000, Schlöder GmbH

Semiconductor Parameter Analyzer:

HP4145B, Agilent Technologies

Digital Multi Meter:

Agilent 34401A, Agilent Technologies



Typical ESD test PCB:

4 Layer PCB stack up with 1.5mm total thickness approx.
15mm track length from pad for ESD Simulator to DUT pad

280um track width

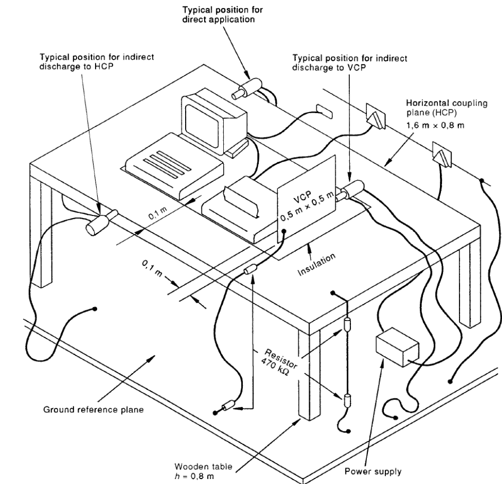
200um spacing

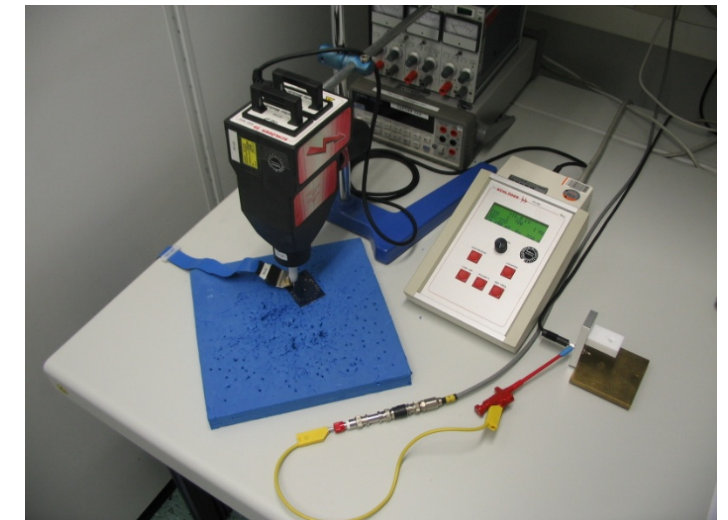
35um Cu thickness

Top layer Cu filled

2nd layer GND plane

GND Via in DUT footprint: 150µm Cu filled





ESD Tolerance Test – Failure testing

After each test level, device characteristics will be checked by comparing initial curve progression vs. actual curve progression

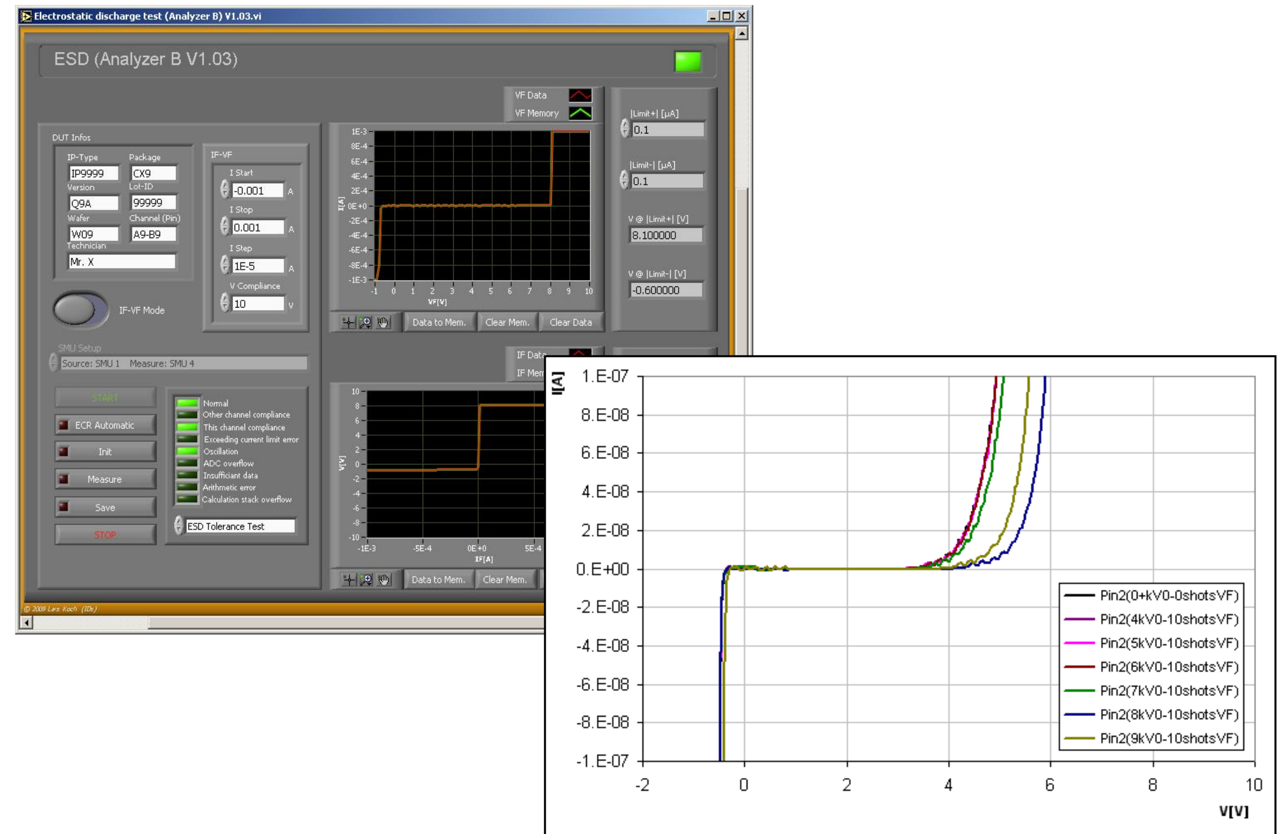
Detection of „fail" DUT by:

- Modified break down voltage
- Higher leakage current
- Changed series resistor
- Abnormal curve progression

For characterization purpose

- Curve progression V = f(I)
- Curve progression I = f(V)

are analyzed and will be stored as MS Excel file



ESD Robustness

ESD Robustness / ESD Rating / ESD Tolerance

- PESD2IVN24-T:

ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2] [3]	-	30	kV
		ISO 10605; contact discharge; C = 330 pF, R = 330 Ω	[2] [3]	-	30	kV
		ISO 10605; contact discharge; C = 150 pF, R = 330 Ω	[2] [3]	-	30	kV

[2] Measured from pin 1 or 2 to pin 3.
[3] Device stressed with ten non-repetitive ESD pulses.

- ESD Robustness of the device alone

→ This value does not allow to draw conclusion about system level ESD robustness

ESD – Clamping Voltage

Clamping voltage V_{clamp} e.g. for 8 kV ESD pulse – PESD2IVN24-T

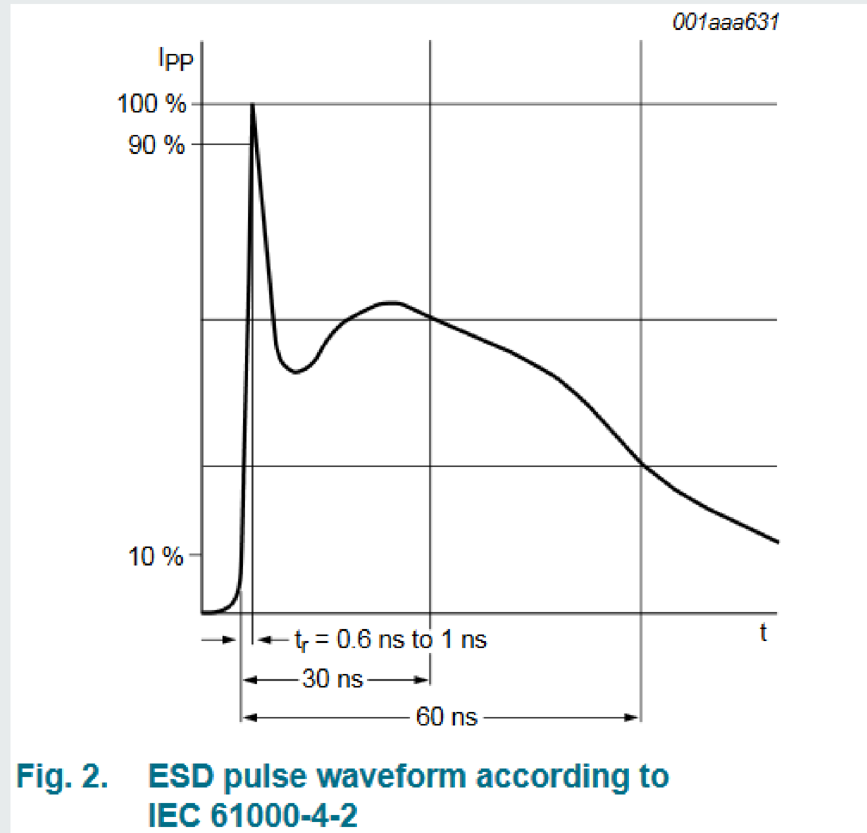


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

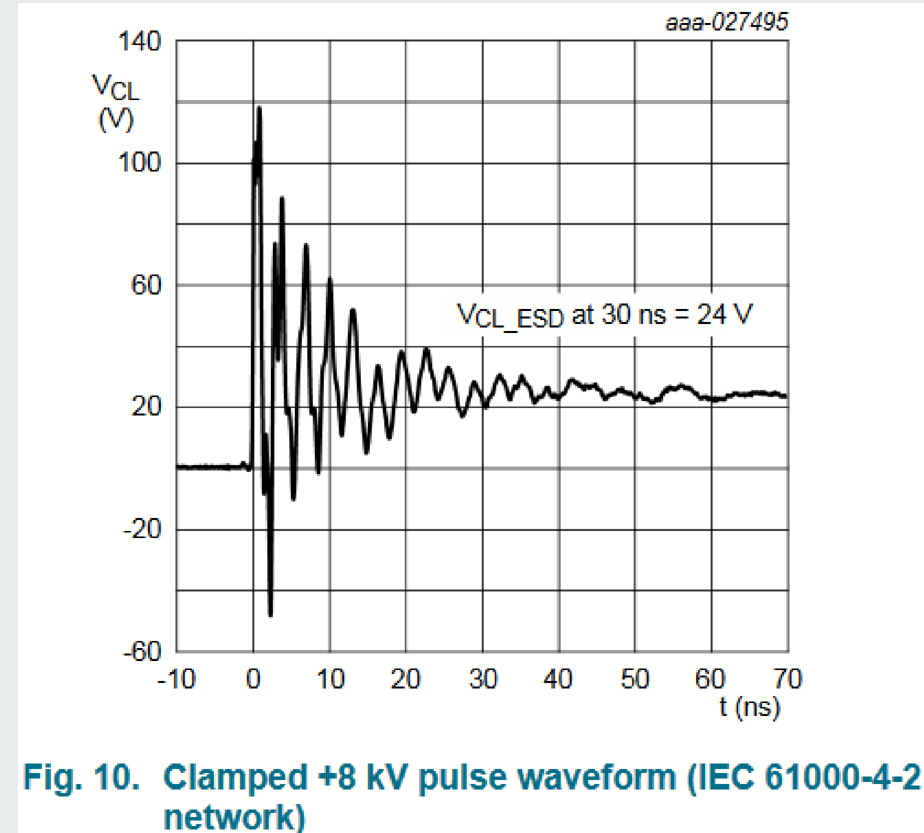
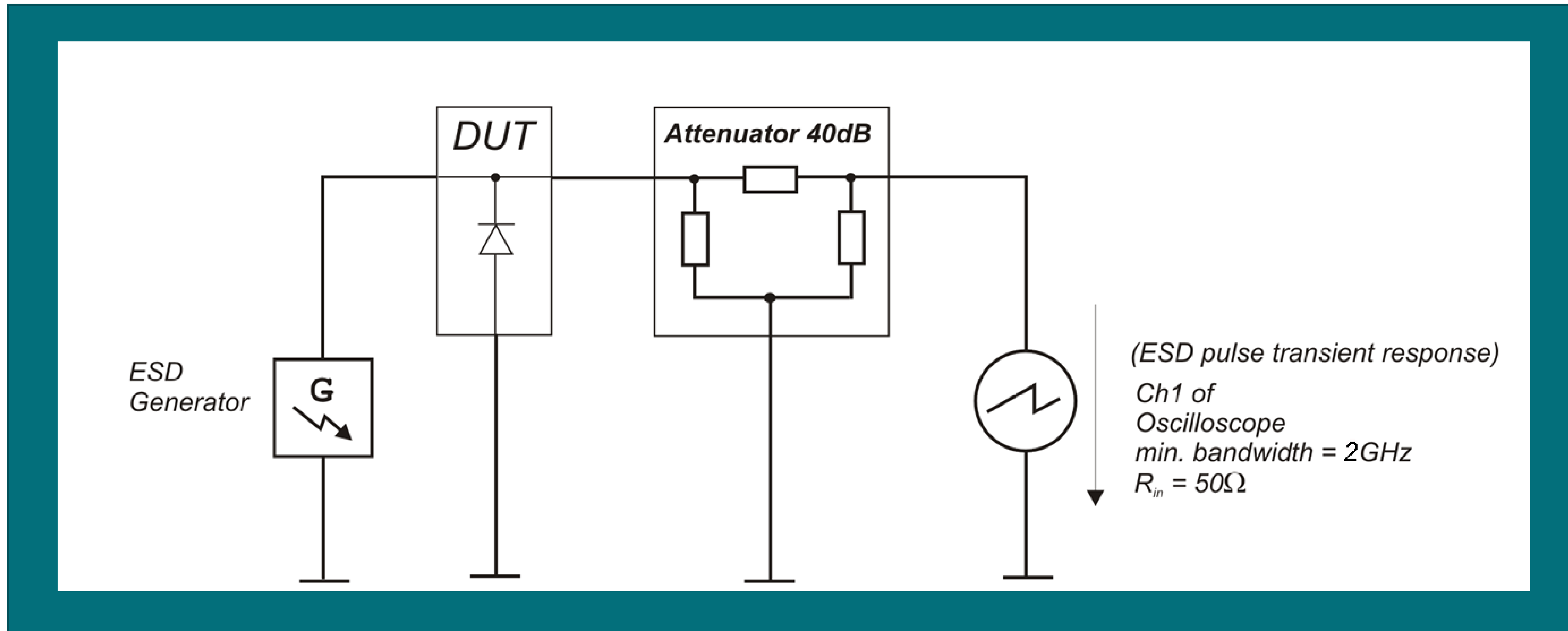


Fig. 10. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

Clamping voltage according to IEC61000-4-2

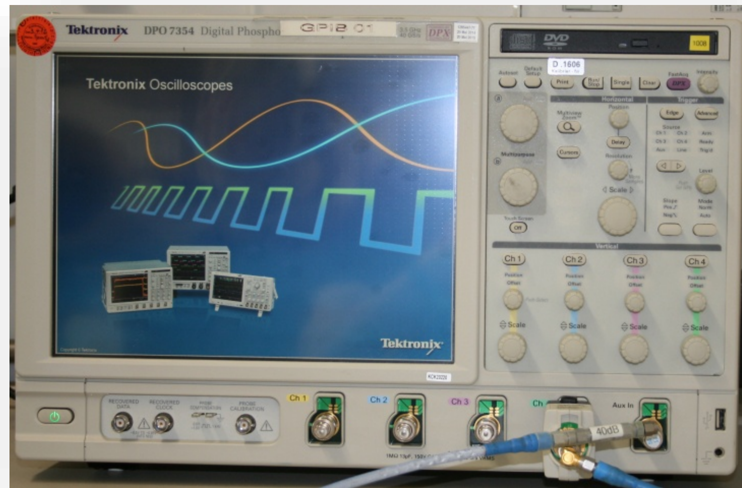


The usage of a high sample rate at the oscilloscope is very important
Measurement with low sample rate can be seen in some datasheets to tune results.

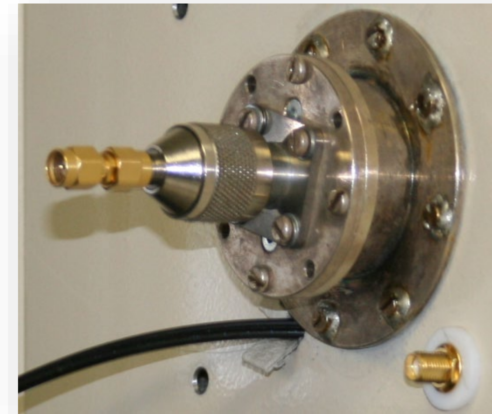
Vcl measurement setup (IEC61000-4-2 wave form)

Connection to DUT and Scope

- SMA connectors
- DUT on PCB with 50 Ohm matched impedance lines
- 40 dB attenuator
- 3.5 GHz Scope (Tektronix DPO 7354)

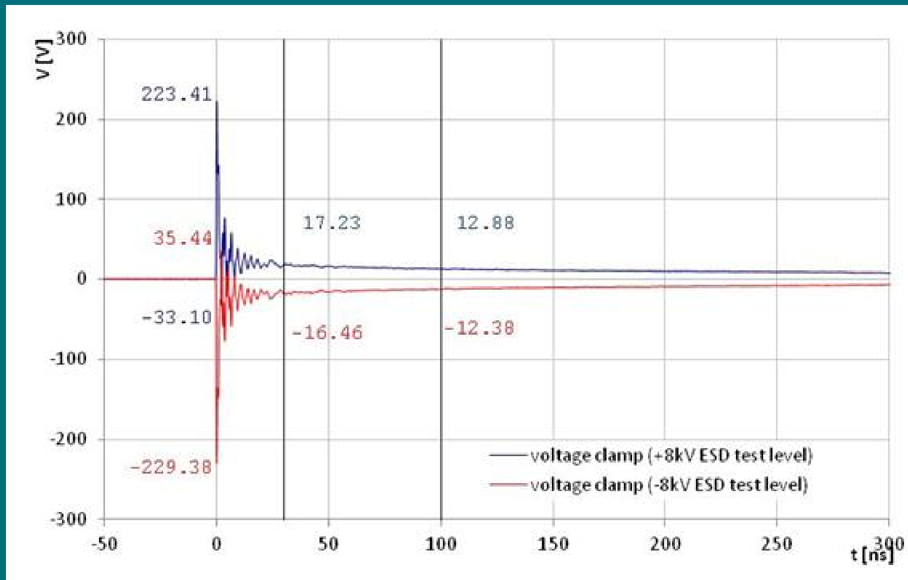


DUT



Clamping voltage: Too low sampling

Measurement of competitor ESD protection devices in Nexperia lab compared to datasheet values



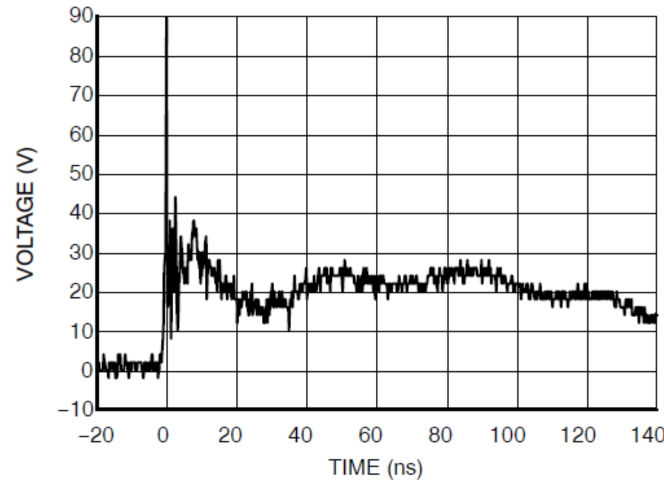


Figure 3. IEC61000−4−2 +8 KV Contact Clamping Voltage

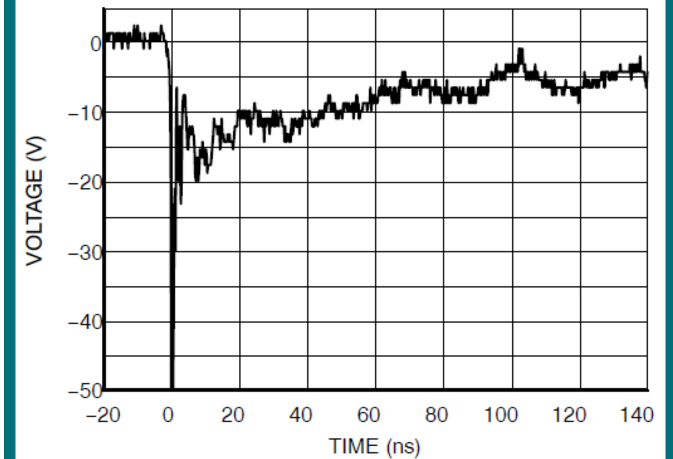


Figure 4. IEC61000−4−2 −8 KV Contact Clamping Voltage

Sampling with a high frequency, at least 2GHz

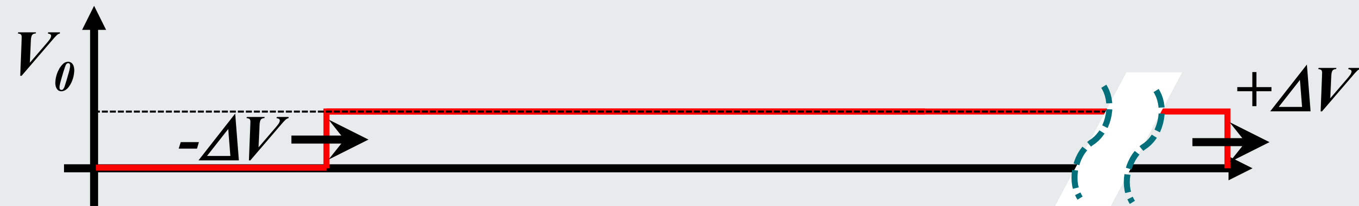
Sampling with a low frequency

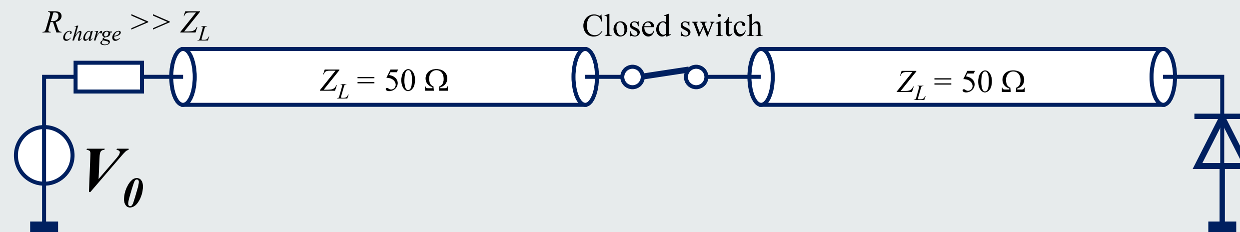
TLP Test

Transmission Line Pulse

- High impedance charge resistor reflects voltage change back into coaxial line

IV





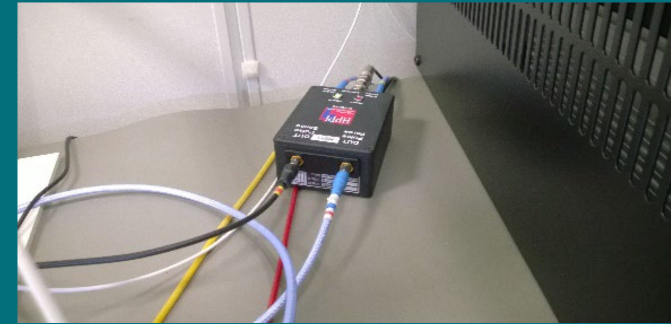
TLP Test – Set up for component testing

HPPI TLP generator

Generator

2 pulse width extender

Switch-box



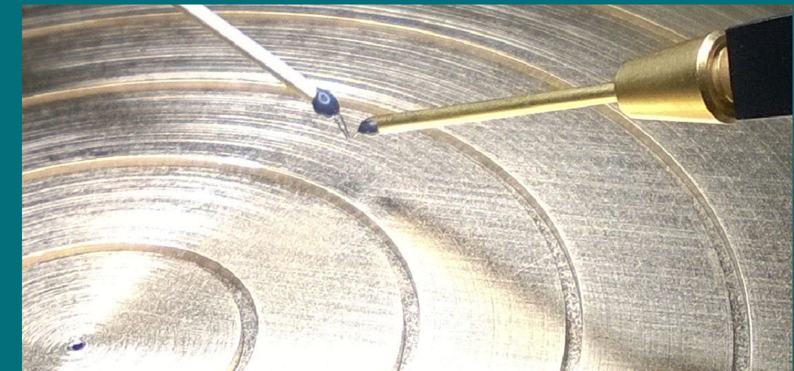
Microscope for needle testing

With micro manipulators

Two needle pairs for powerless sense

Needle probes

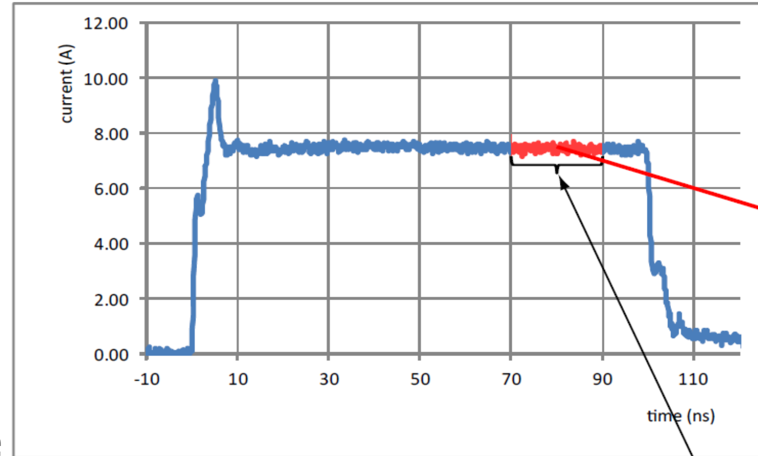
DUT is put backside down on an ceramic insulator tile. The 2 needle pairs are contacted directly (signal pad; ground pad)

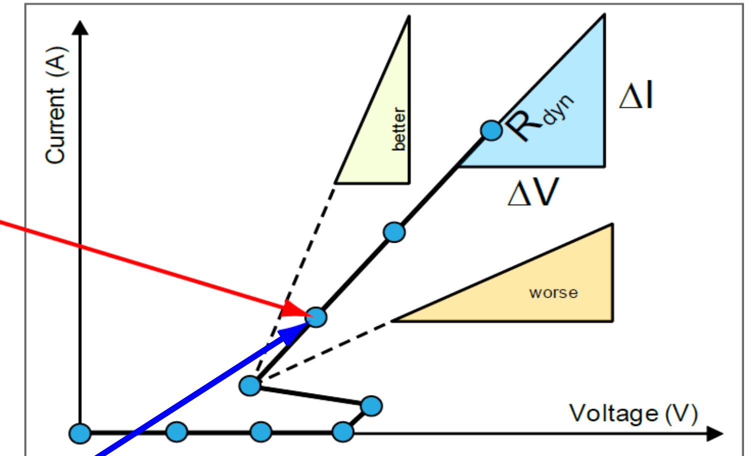


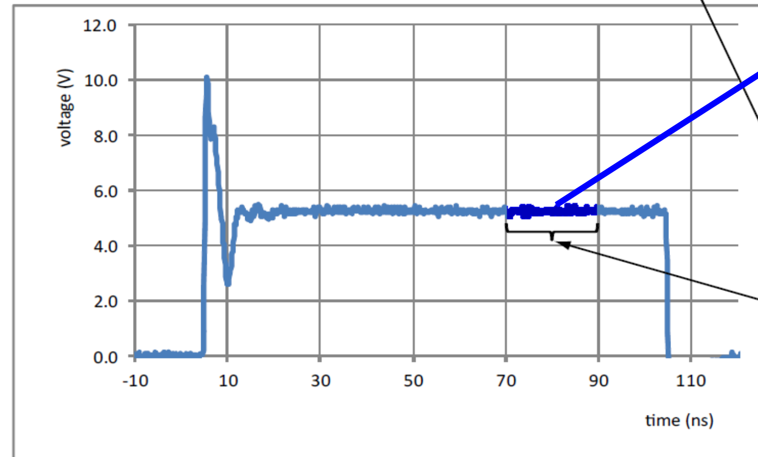
TLP Test

Transmission Line Pulse

- Typical pulse width 100 ns
- VF-TLP (very fast) ~3 ns
- Number of pulses with increased voltage
- Every pulse leads to an measurement point in IV curve



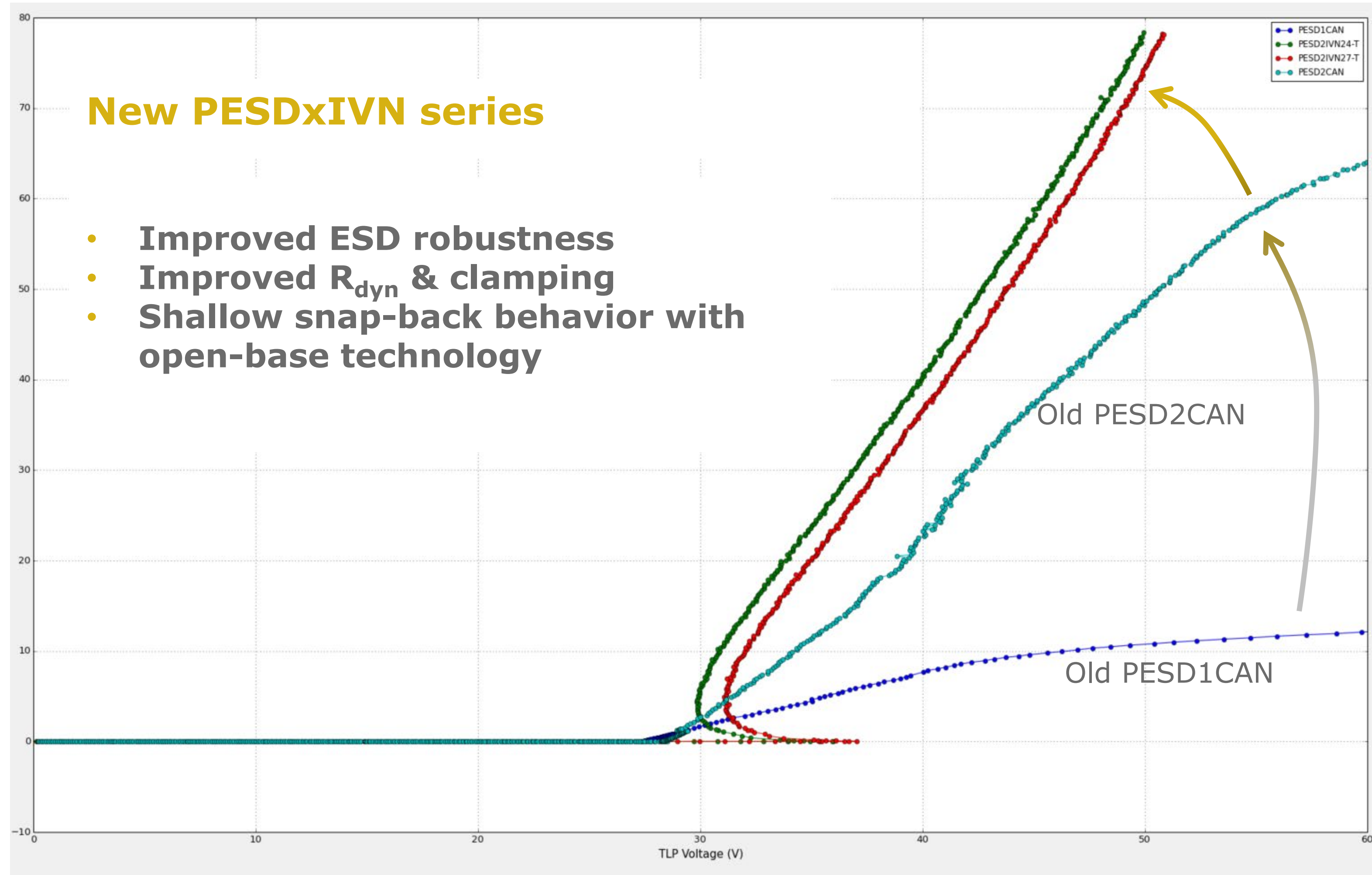




The dynamic resistance R_{dyn} is derived from the steepness of the TLP graph: $\Delta V / \Delta I$

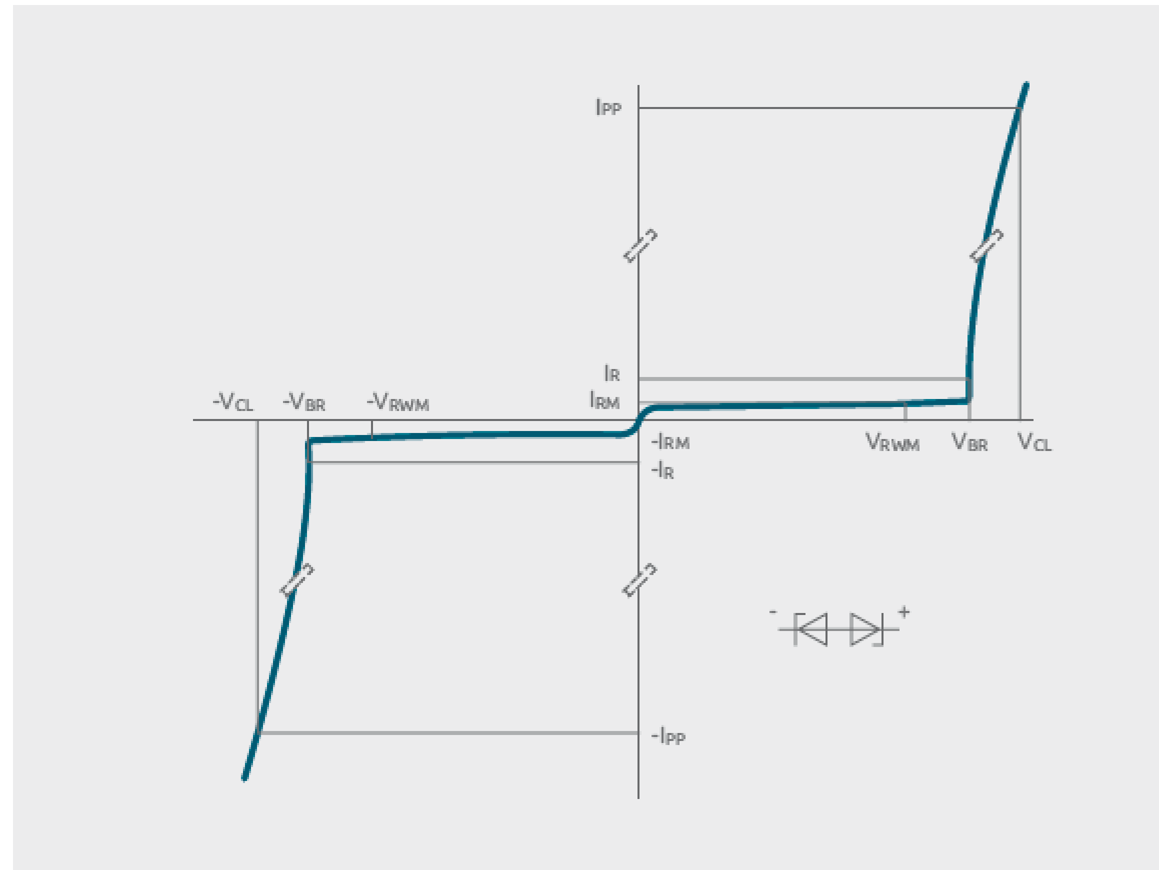
For each TLP measurement voltage and current samples are averaged over 20 ns and denoted as single point in the TLP graph.

TLP Graphs Comparison



Characteristics of ESD Protections

Classical Zener Characteristic



V_{RWM}: Reverse standoff voltage
V_{BR}: Breakdown voltage
V_{CL}: Clamping voltage
I_{RM}: Maximum reverse current
I_{PP}: Maximum surge current

company confidential

Characteristics of new ESD Protections

Snap Back

V_{RWM}: Reverse standoff voltage
V_{BR}: Breakdown voltage
V_{CL}: Clamping voltage
I_{RM}: Maximum reverse current
I_{PP}: Maximum surge current

V_t: Trigger voltage
V_h: Holding voltage

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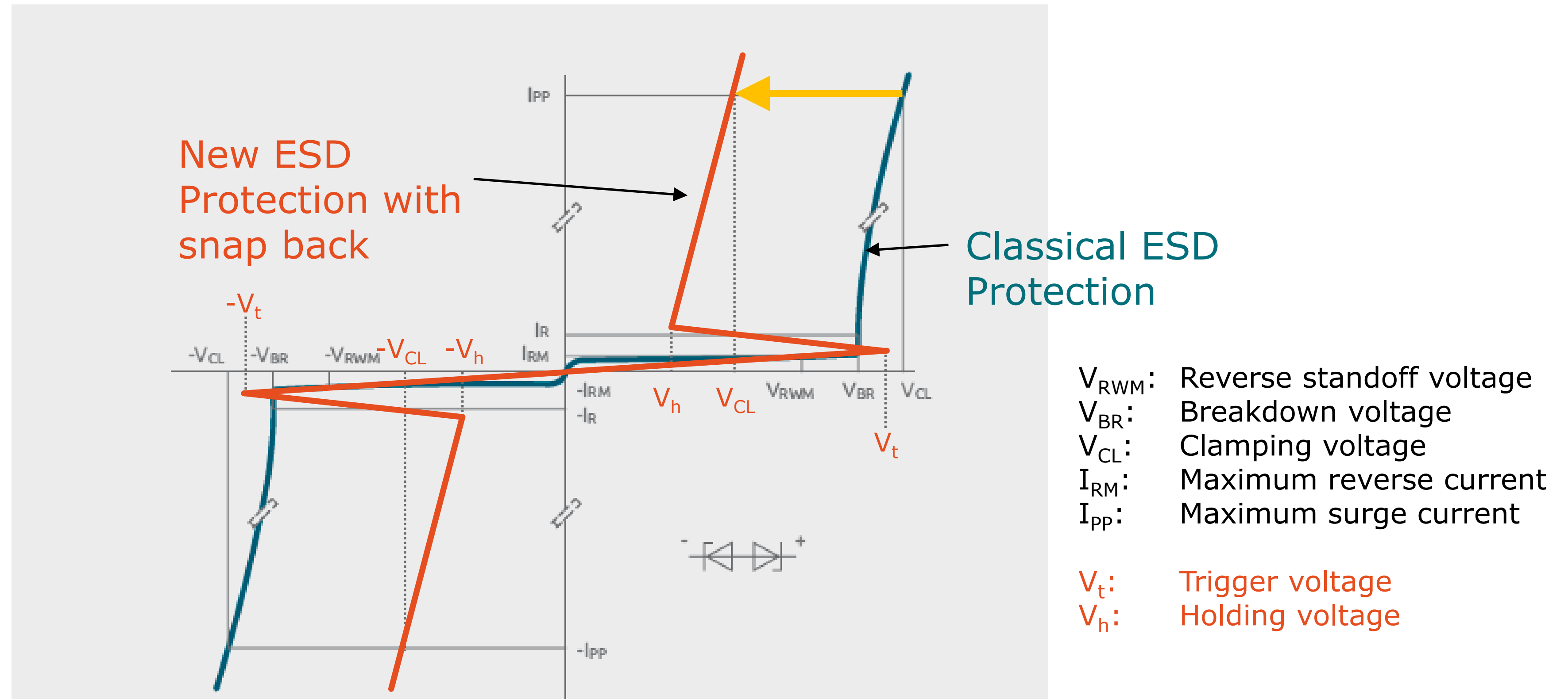
Characteristics of new ESD Protections

Snap Back



Reducing V_{CL} -> Improving Robustness of the PHY

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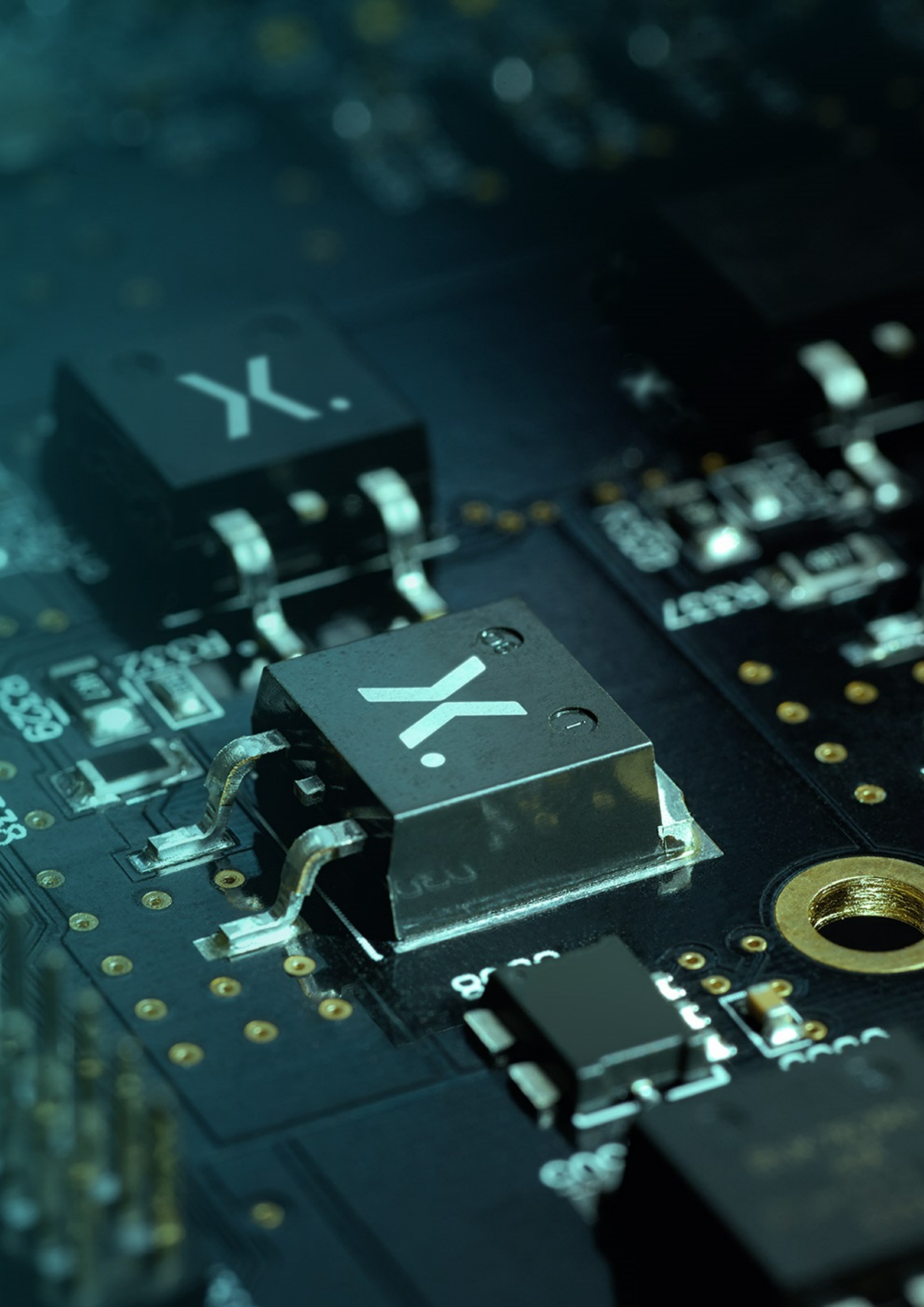


ESD Seminar Session 1

Agenda

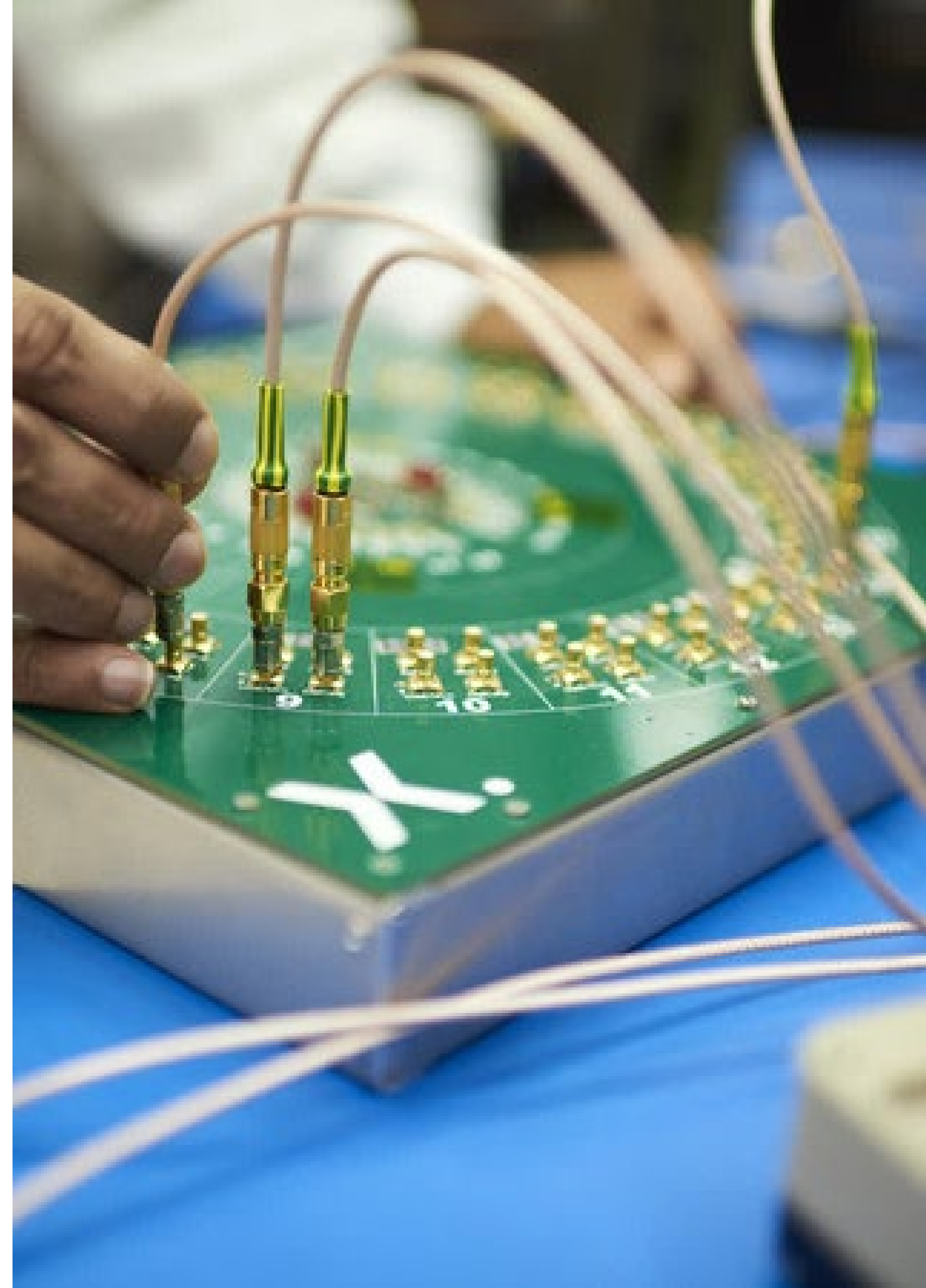
- Fundamentals of ESD Protection
- Measurement and Characterization
- **Nexperia Lab**
- Q&A

Nexperia Lab

Only on customer request

With our dedicated team we offer a broad variety of design support. This includes:

- Design review and error tracking from application to device level
- Analysis tools
- Device characterization with TLP measurements
- PCB screening with EMI scanner
- SEED modelation and simulation
- S-Parameters, (RF)-SPICE models and others

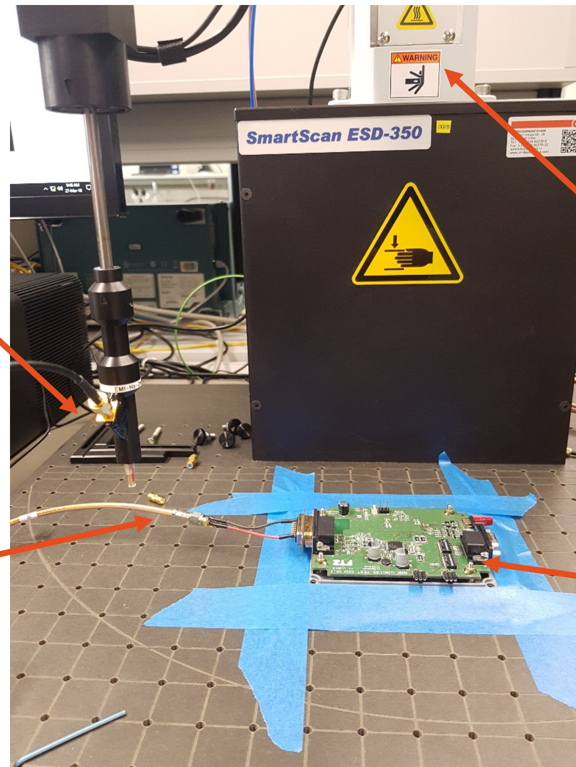


EMI - Scanner

To measure how the ESD pulse distribute across the PCB

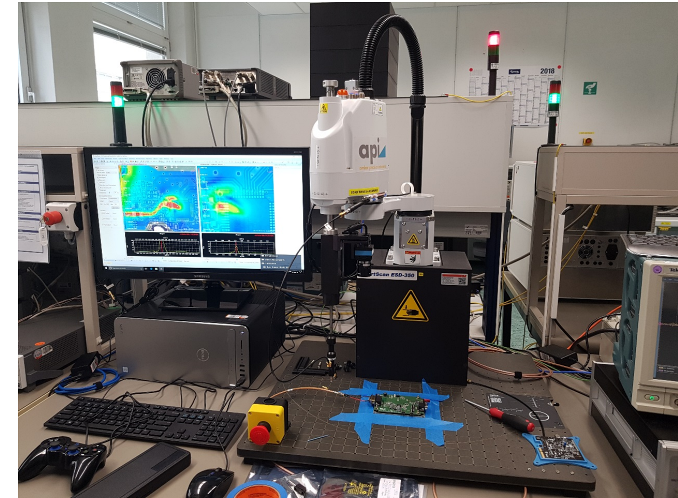
H-Field Probe

Pulse feed



Robotic arm

DUT (PCB)



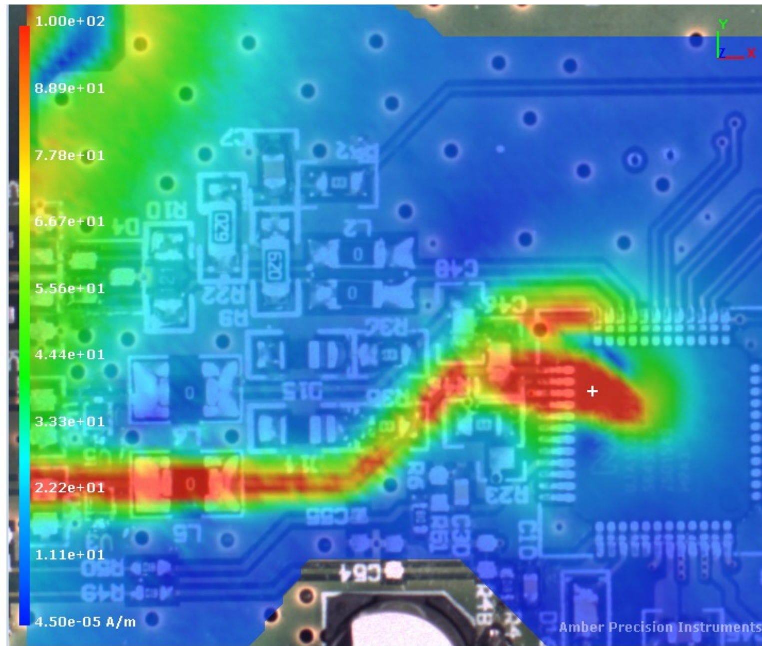
Pulse generator

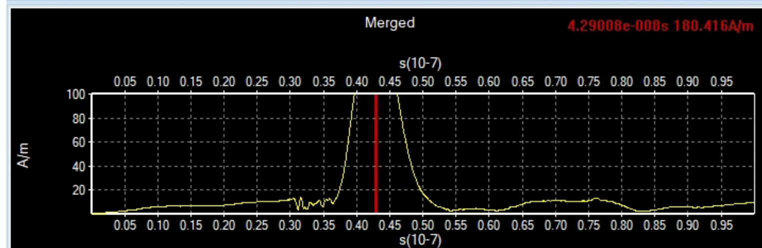
EMI - Scanner

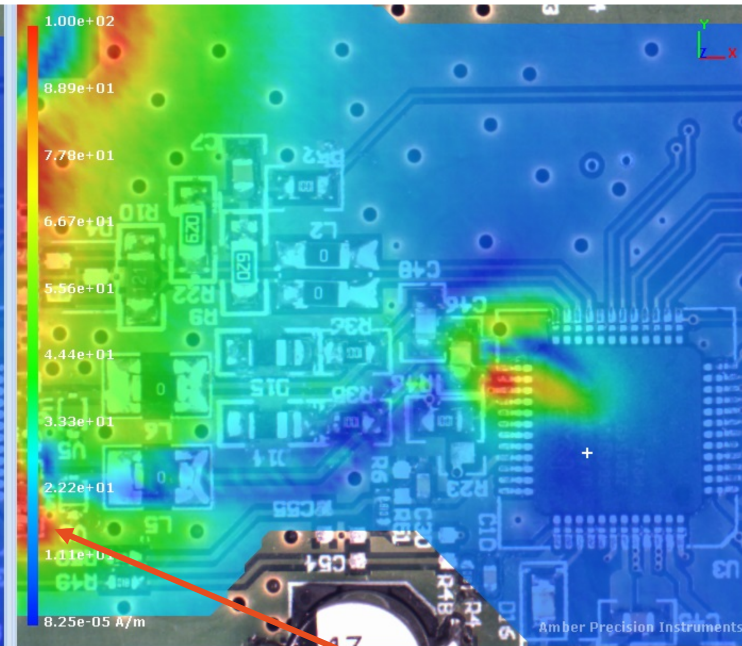
To measure how the ESD pulse distribute across the PCB

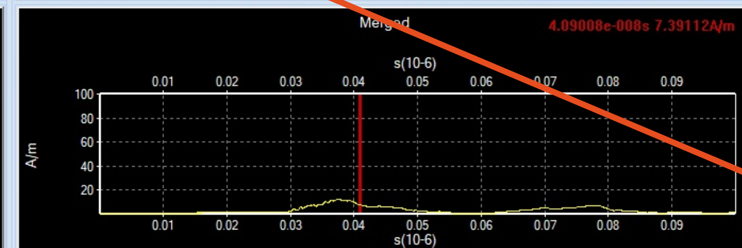
CAN Transceiver reference board

Without protection









With protection

PESD2IVN24-T

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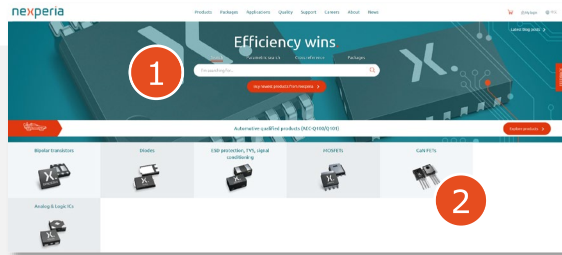

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www.nexperia.com

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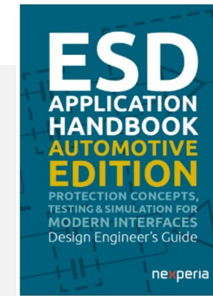
  - Parametric Search
  - Package Search
- 2
  - Product Overview
    [Path to Datasheets, Product Brochures, Application Examples, …]

Documentation Center

Link Selection Guide

- Overview on all our Discrete, Logic and MOSFET devices
  - Diodes & Transistors
  - **Protection & Filtering**
  - MOSFETs
  - Logic
  - Packages



Application Handbook

Link ESD

- Automotive interfaces and applications
- Testing standards
- Simulation methods
- English & Chinese version
- PDF & Hardcopy

Lab support

- Dedicated engineering team to support customer requests
- Solution investigation with various analysis tools especially
- TLP, EMI scan, SEED
- Contact us for details

Q&A

ESD for Electronic Design Engineers Seminar

nexperia

EFFICIENCY WINS.

Photo: RichVintage / Getty Images

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