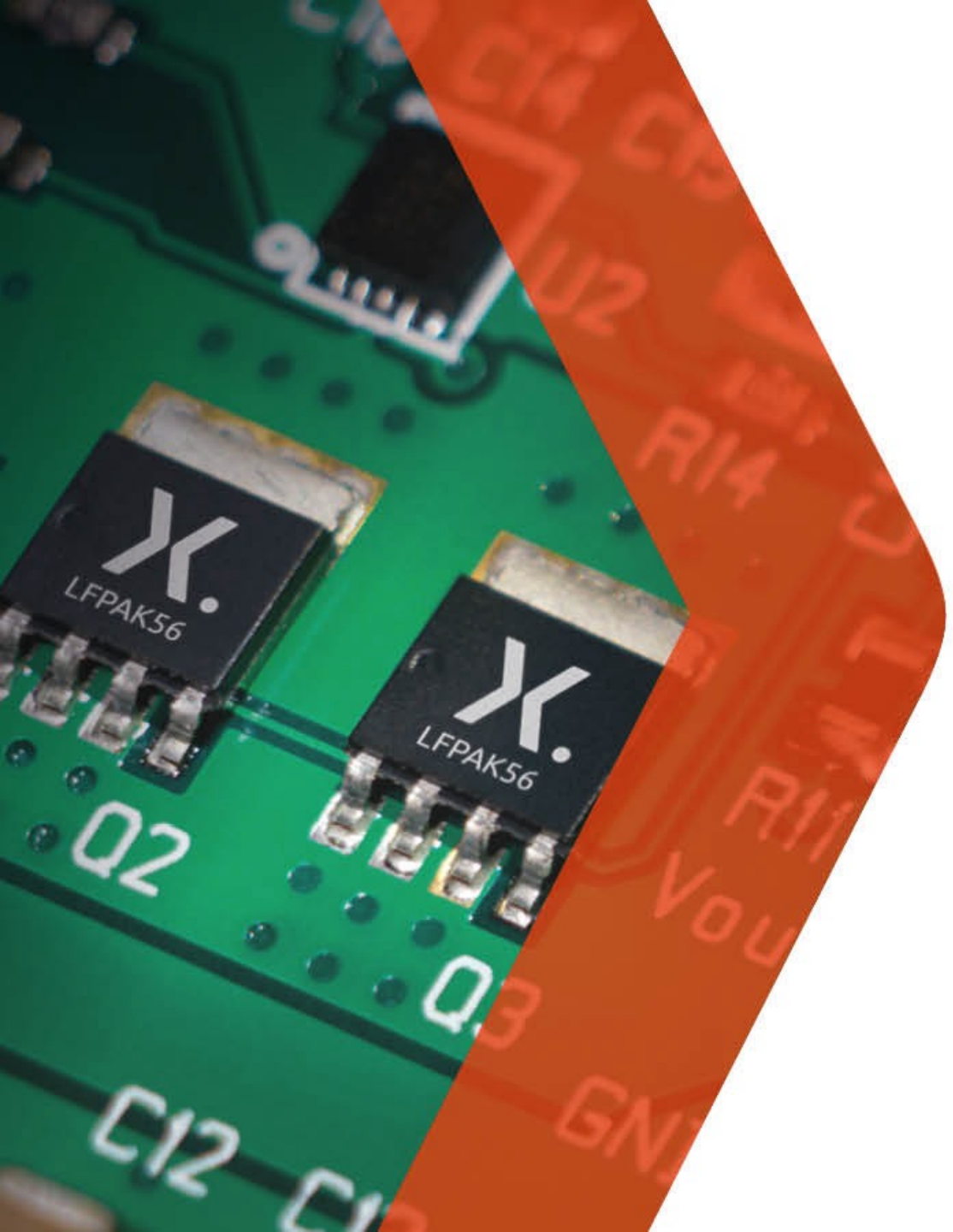


nexperia

New CCPAK double pulse evaluation board

Power GaN FETs

September 2021

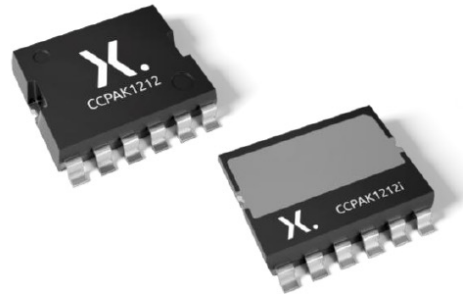
Introduction

- Sebastian Klötzer
- Principal Application Engineer

- Giuliano Cassataro
- GaN Marketing & Commercial Director

Outline

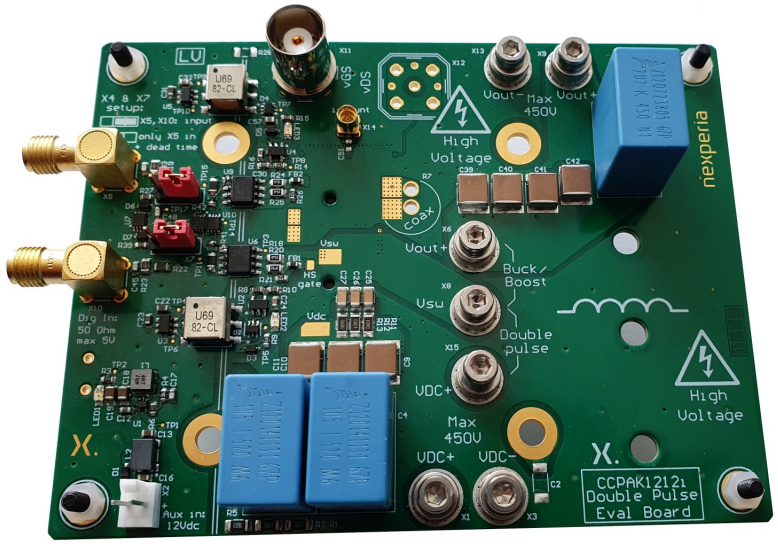
Featured Product	Description
GAN039-650NxB(A)	650V, 33mΩ GaN FET in CCPAK, H2 Technology



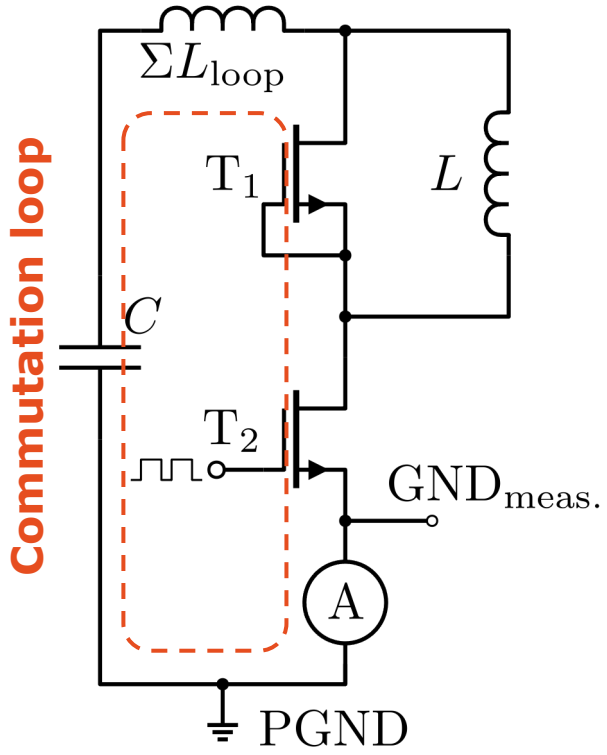
- Benchmarking fast GaN devices in double pulse is a challenging task that requires a specifically tailored PCB.
- The PCB must enable high bandwidth current measurement while keeping parasitics to a minimum

Features of the new evaluation board for GaN devices in CCPAK:

- Half-bridge with very low commutation inductance
- High bandwidth low-side current measurement
- Fixed measurement access for low distortion and repeatability
- Capability to evaluate thermal performance (R_{th}) and continuous operation



Main function: Double pulse test

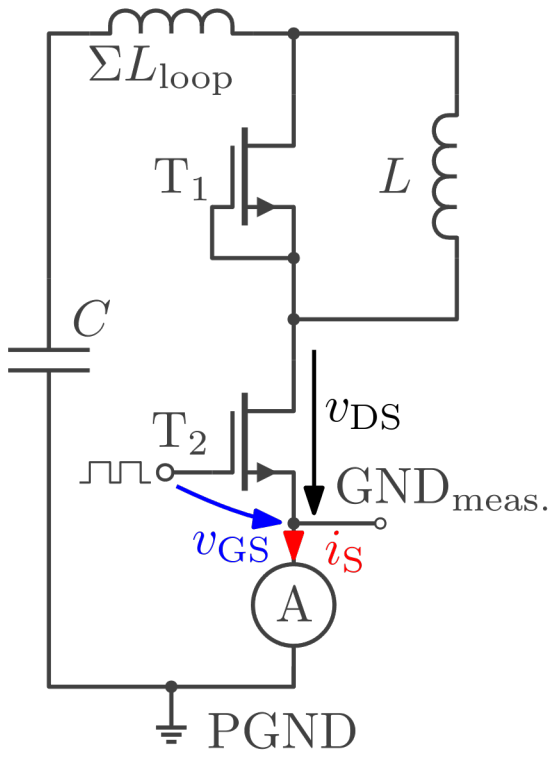


Half-bridge with current measurement

- Standard method to evaluate hard-switching performance such as
  - Switching losses (E_{on}, E_{off})
  - Current and voltage slopes (dv/dt, di/dt)
  - Reverse-recovery behaviour (Q_{rr})
  - Gate drive performance
- Typically performed in a half-bridge setup
- Requires a current sensor in the commutation loop
- All components in the commutation loop contribute to ΣL_{loop}

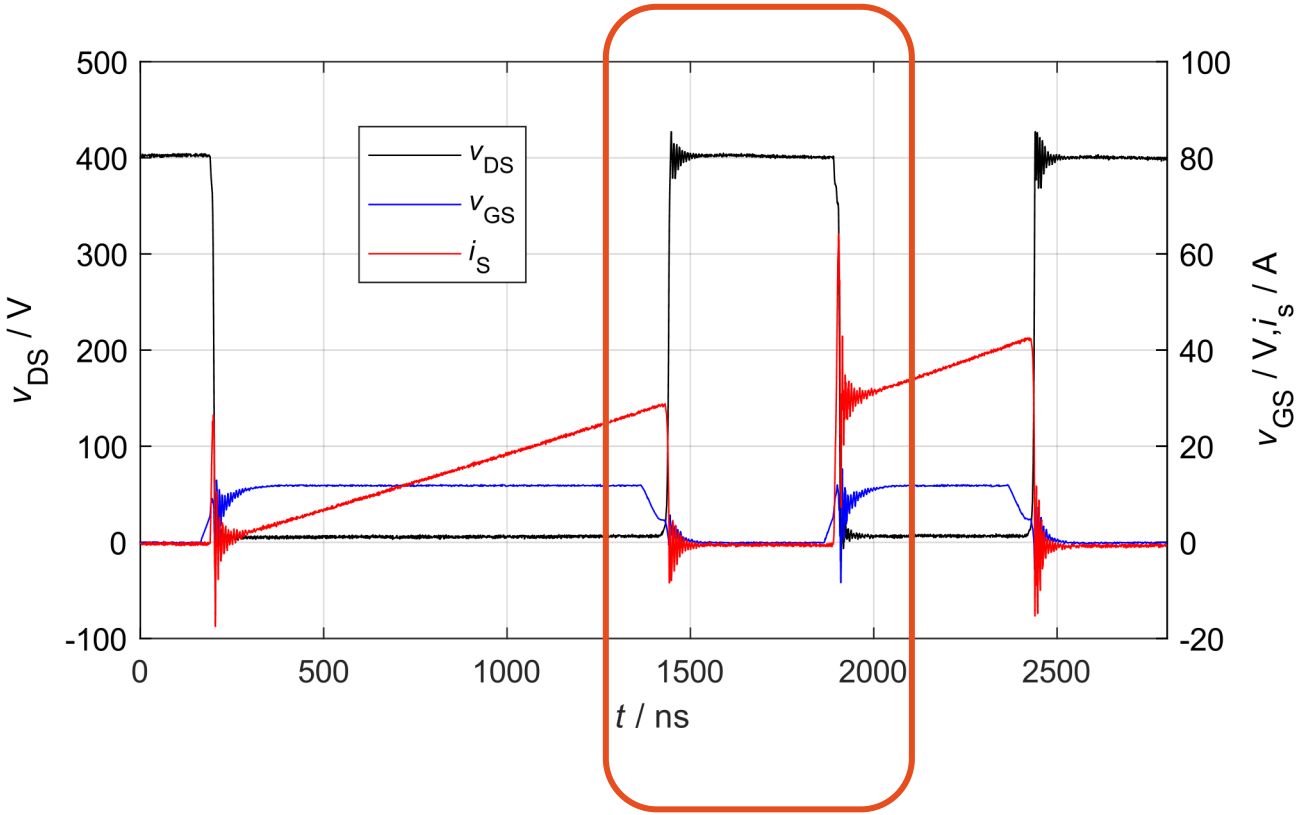
Main function: Double pulse test

Active (low-side) transistor T_2 is turned-on (and off) twice



Half-bridge with current measurement

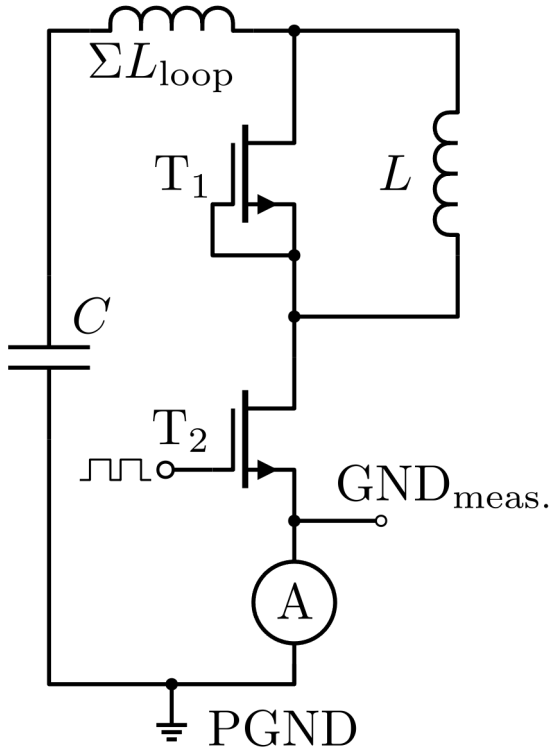
***GND_{meas}: reference point for scope**



Turn off and turn on at the same current

→ Desired test currents are set by variation of gate drive pulse lengths

Main function: Double pulse test



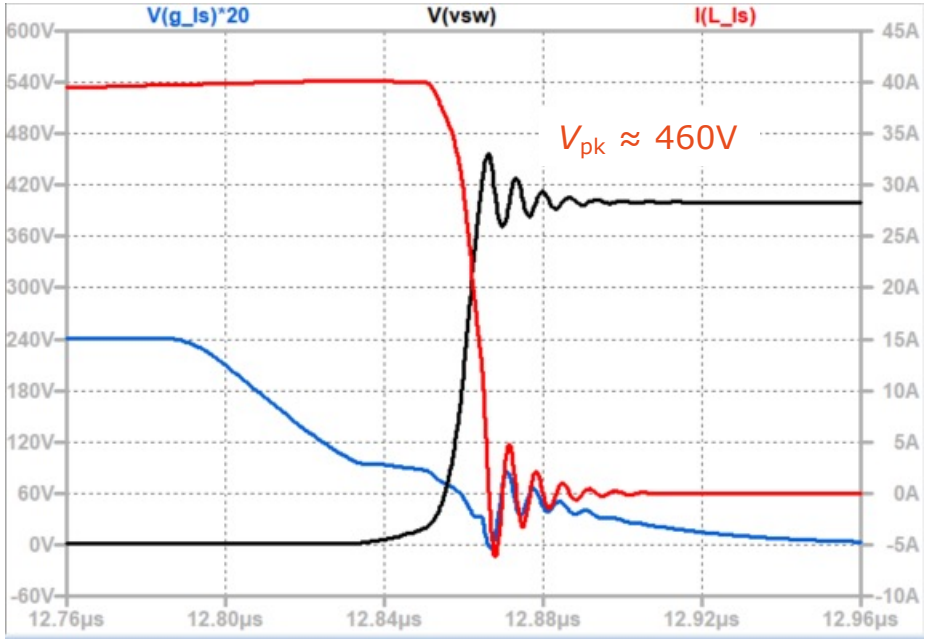
Half-bridge with current measurement

Requirements for good double pulse test performance:

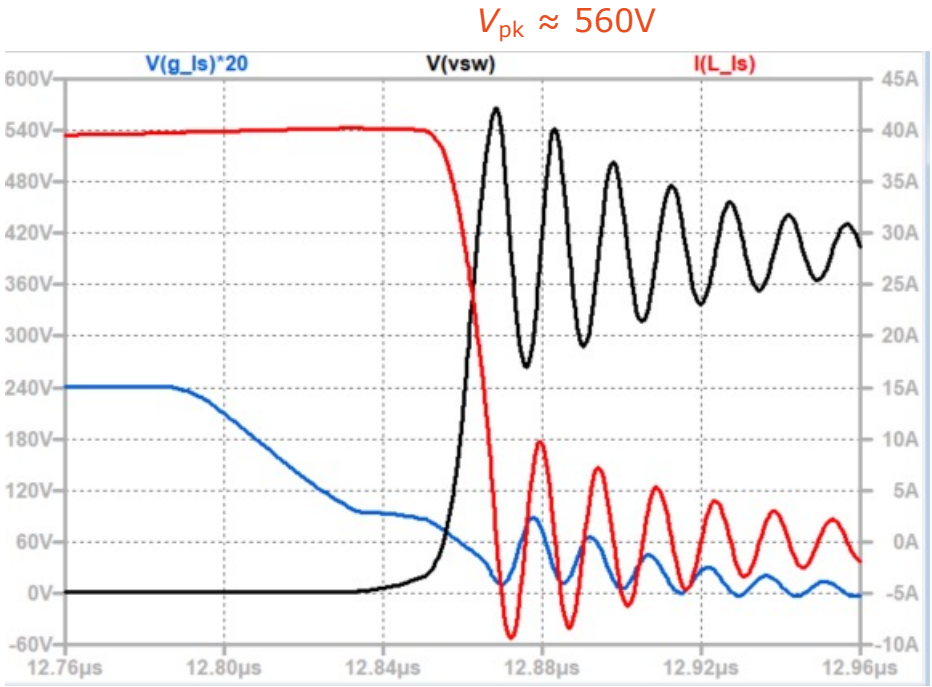
1. Minimization of power loop parasitics:
   Mainly ΣL_{loop} but also switch-node and inductor winding capacitances
2. Minimization of the gate loop parasitics
3. Ensuring high bandwidth measurement with low distortion

Impact of ΣL_{loop}

- Loop inductance has a big impact on results
- Rule of thumb for copper wire: 10 nH/cm!
- Simulation of GAN039:

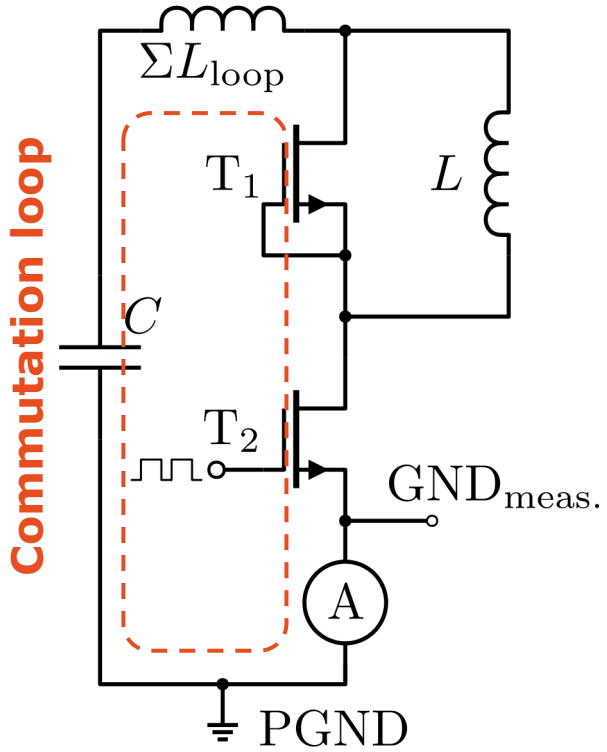


Decent design: 10nH total loop inductance



Mediocre design: 30nH total loop inductance

Commutation loop inductance ΣL_{loop}



Half-bridge with current measurement

Contributors to ΣL_{loop}:

- Power semiconductors
- DC-Link capacitor
- PCB layout
- Current sensor

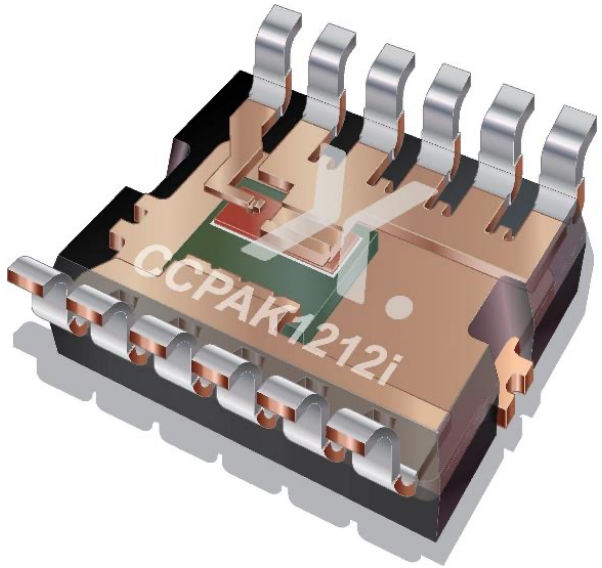
Also part of final design

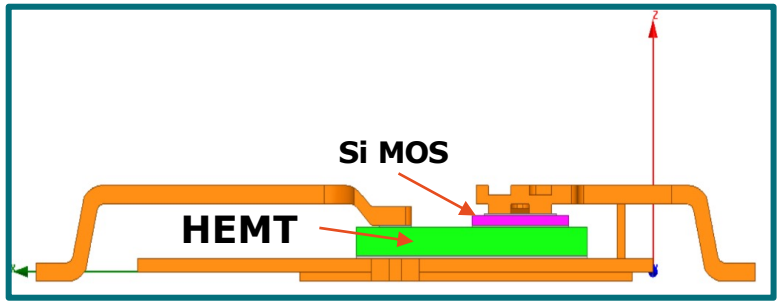
Part of evaluation setup
→ Highest resolution of current at minimum impact on design required

Commutation loop inductance ΣL_{loop}

Contributors to ΣL_{loop}:

- **Power semiconductors**
- DC-Link capacitor
- PCB layout
- Current sensor



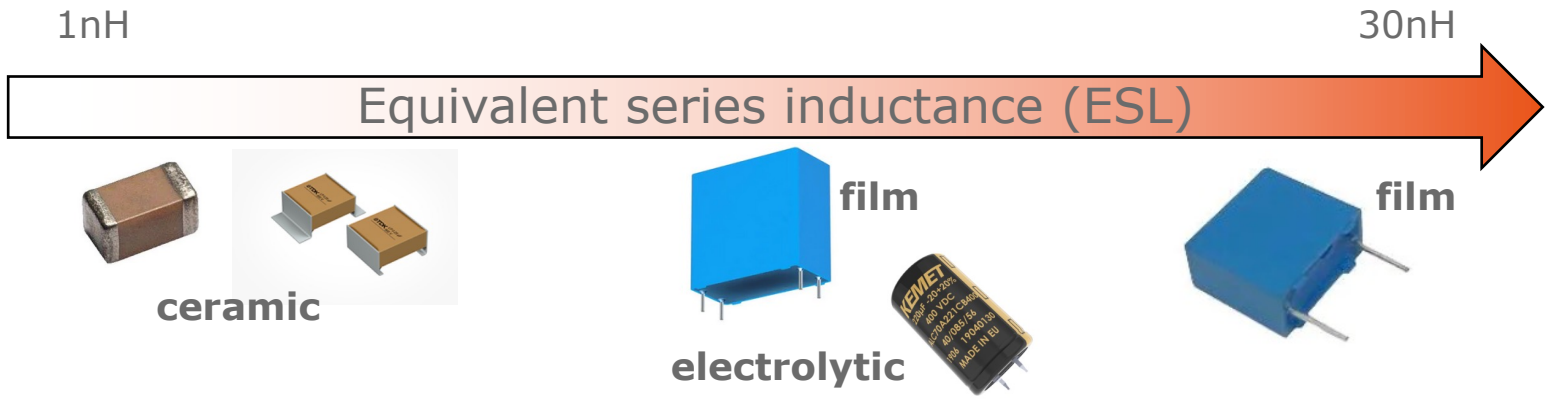


- Can be the main contributor to ΣL_{loop}
- Advantage for clip-bonded SMD packages such as CCPAK: L ca. 2nH
- In comparison: TO-247: ca. 10nH

Commutation loop inductance ΣL_{loop}

Contributors to ΣL_{loop}:

- Power semiconductors
- **DC-Link capacitor**
- PCB layout
- Current sensor



➢Best switching performance: SMD ceramic capacitors (MLCCs)

➢Both film and electrolytic caps work well in various applications

but: there should always be at least one MLCC directly at the half-bridge for best switching performance

Commutation loop inductance ΣL_{loop}

Contributors to ΣL_{loop}:

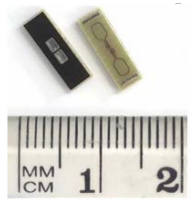
- Power semiconductors
- DC-Link capacitor
- PCB layout
- **Current sensor**

10s MHz — GHz

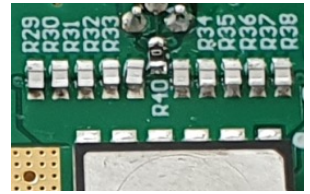
Bandwidth

Rogowski coil

Current transformer



Field sensor



Spec. SMD shunt design

Coax Shunt

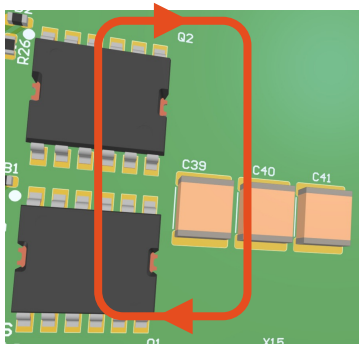
- All methods have advantages and drawbacks
- On the eval. board, we use a custom 47 mΩ SMD shunt array:
  - Very low inductance
  - High bandwidth »100 MHz
  - Easy to use on-board solution

Commutation loop inductance ΣL_{loop}

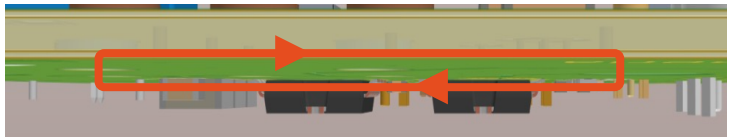
Both horizontal and vertical commutation loop can work well:

Contributors to ΣL_{loop}:

- Power semiconductors
- DC-Link capacitor
- **PCB layout**
- Current sensor

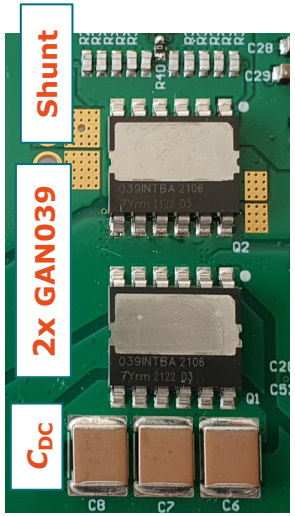


horizontal: loop on single layer

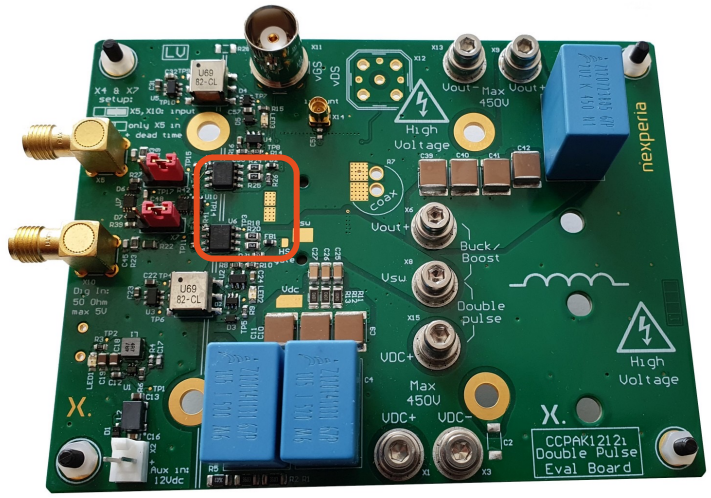


vertical: opposing currents on adjacent layers

- Bottom side cooled devices: horizontal loop often easier
- Top side cooled devices: Full design flexibility, very good vertical commutation loop can be achieved
- Careful layout required to not introduce excessive switch-node capacitance
- Eval. board: Vertical loop, ΣL_{loop} ca. 5 nH



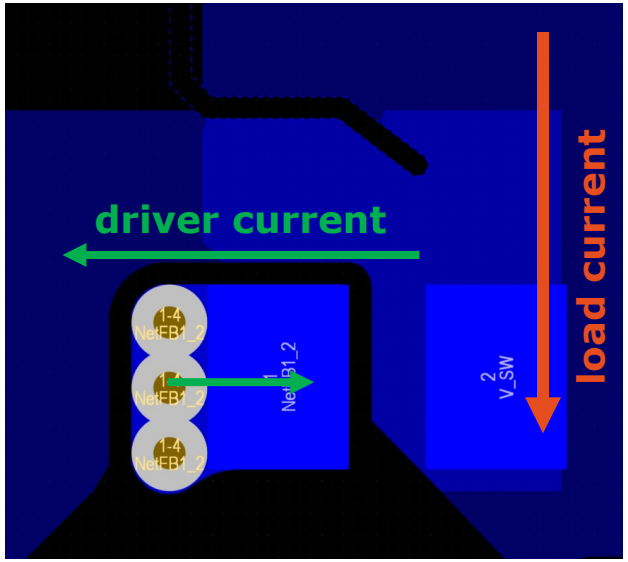
Gate drive requirements



- Cascode GaN has high V_{th}=4 V and rugged FET gate
  - → Standard MOSFET gate driver with 0 V…10-12 V can be used
- CMTI of 100 V/ns is recommended
- Ferrite bead is should be used for stable operation
- High-side supply via bootstrap circuit or isolated supply will both work well

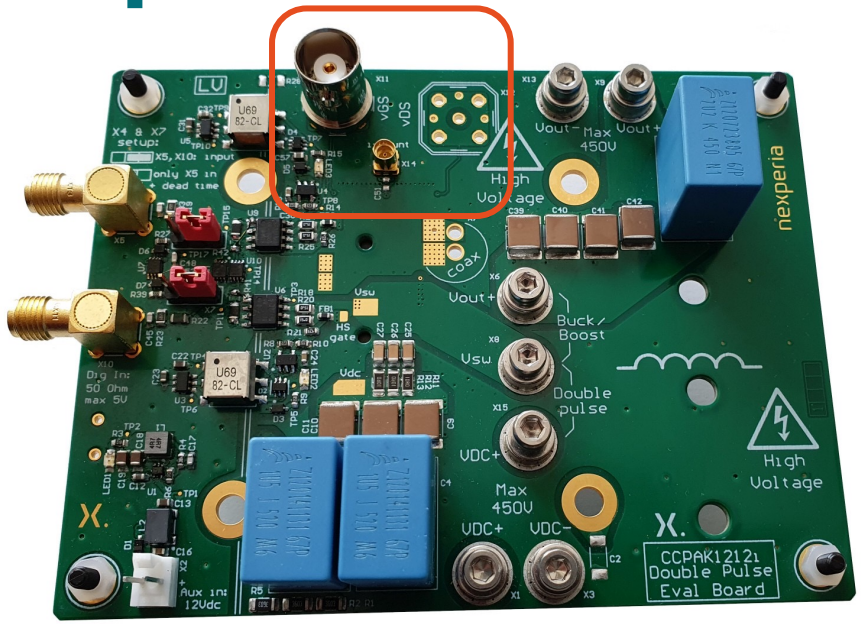
Layout recommendations:

- Aim for very low gate loop inductance
- Minimize switch node size and overlap with DC power rails
- Separate power loop and driver loop - routing on PCB should be similar to a Kelvin-Connection



Measuring waveforms for double pulse

- For low-side measurement: Fixed measurement access options to directly connect low capacitance passive proves
- Avoids long measurement leads, that can introduce ringing and distortion



- Repeatability is important to clearly see impact of modifications (e.g. R_g)
- High-side can be measured (e.g. IsoVu) but does not have fixed nodes on the eval board to prevent connection errors

What you need to test

Minimal lab setup:

<u>For Double pulse:</u>

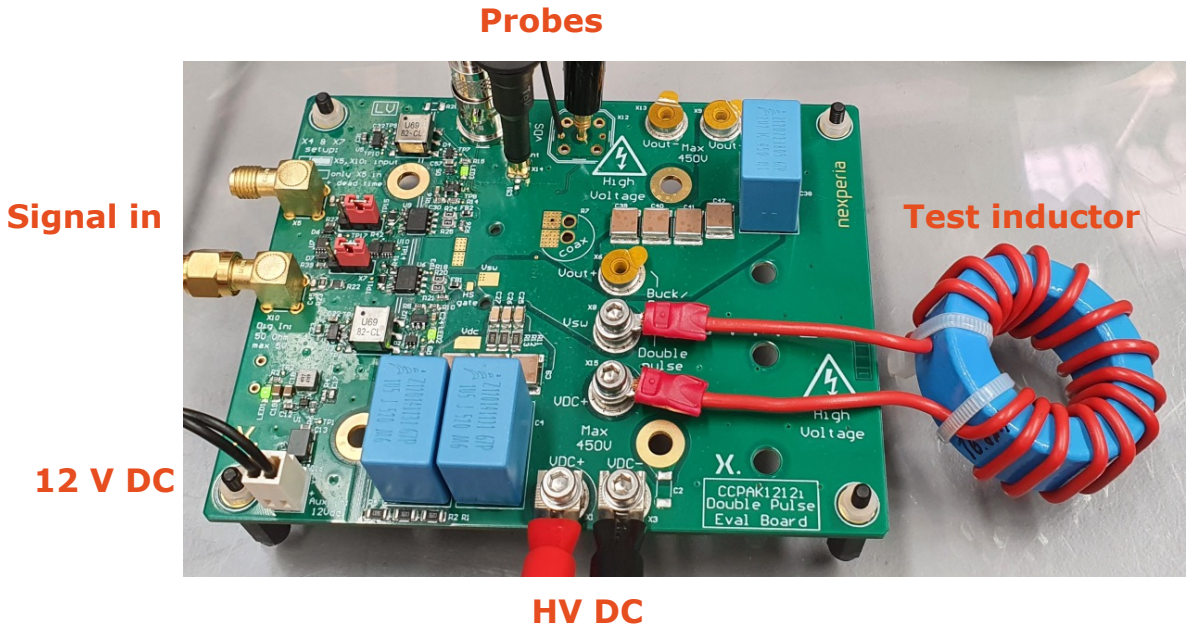
- HV DC source
- 12 V AUX DC source
- Pulse generator, 1 or 2 channel
- Oscilloscope with LV probe, HV probe, coax cable for current measurement

<u>For R_{th} measurement:</u>

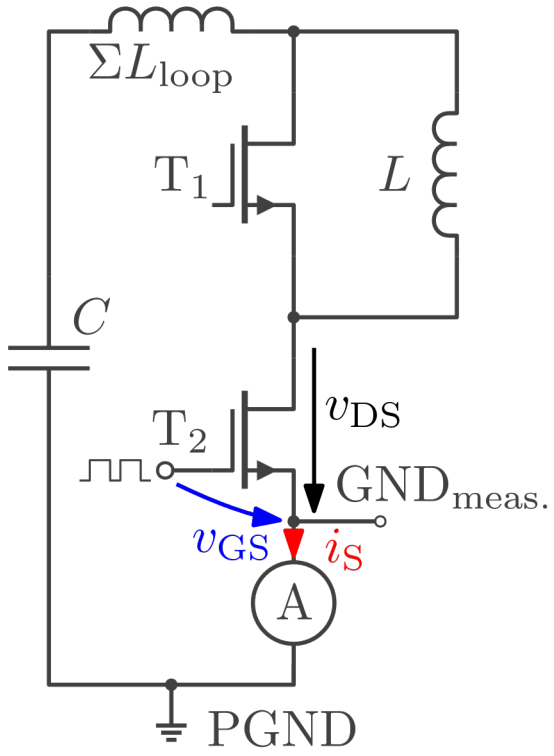
- IR Camera

<u>For Efficiency measurement (continuous operation):</u>

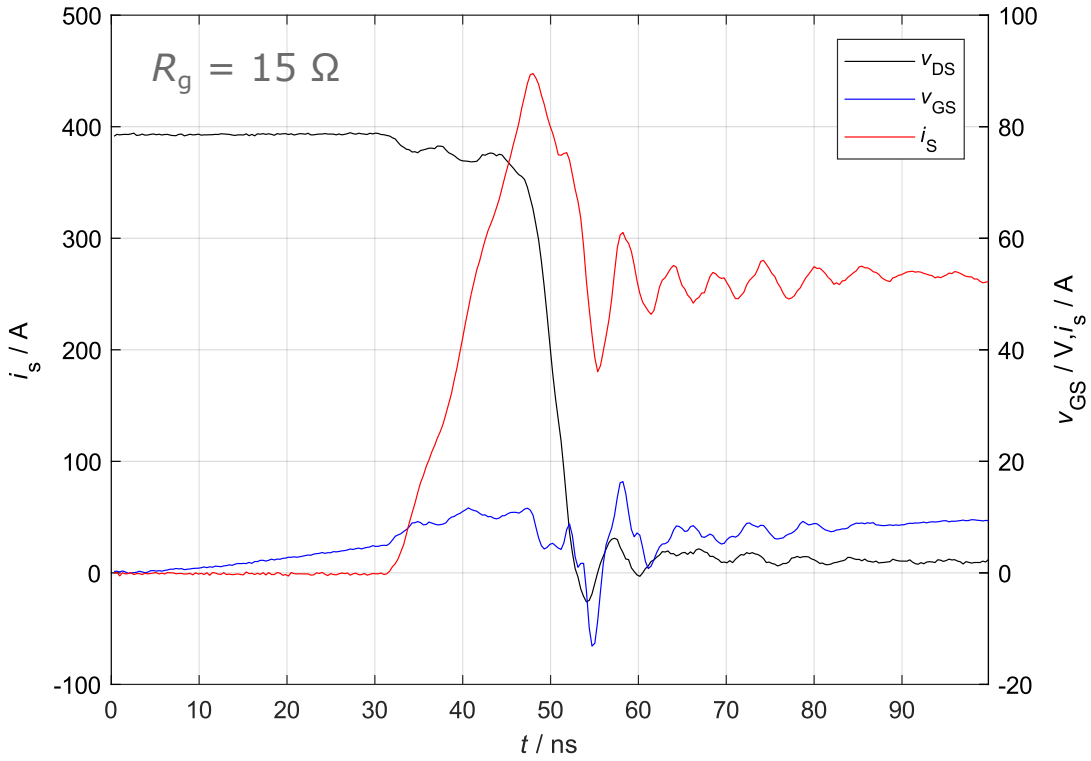
- DC Source & Load, Power Analyzer



Double pulse results



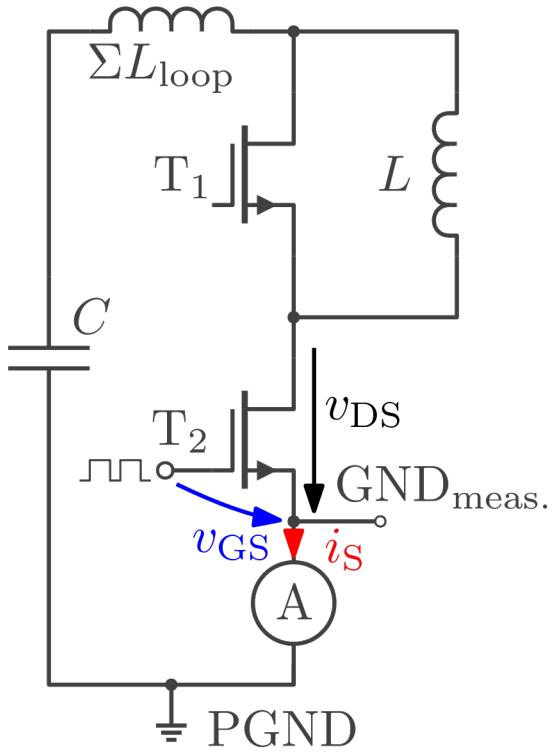
Half-bridge with current measurement



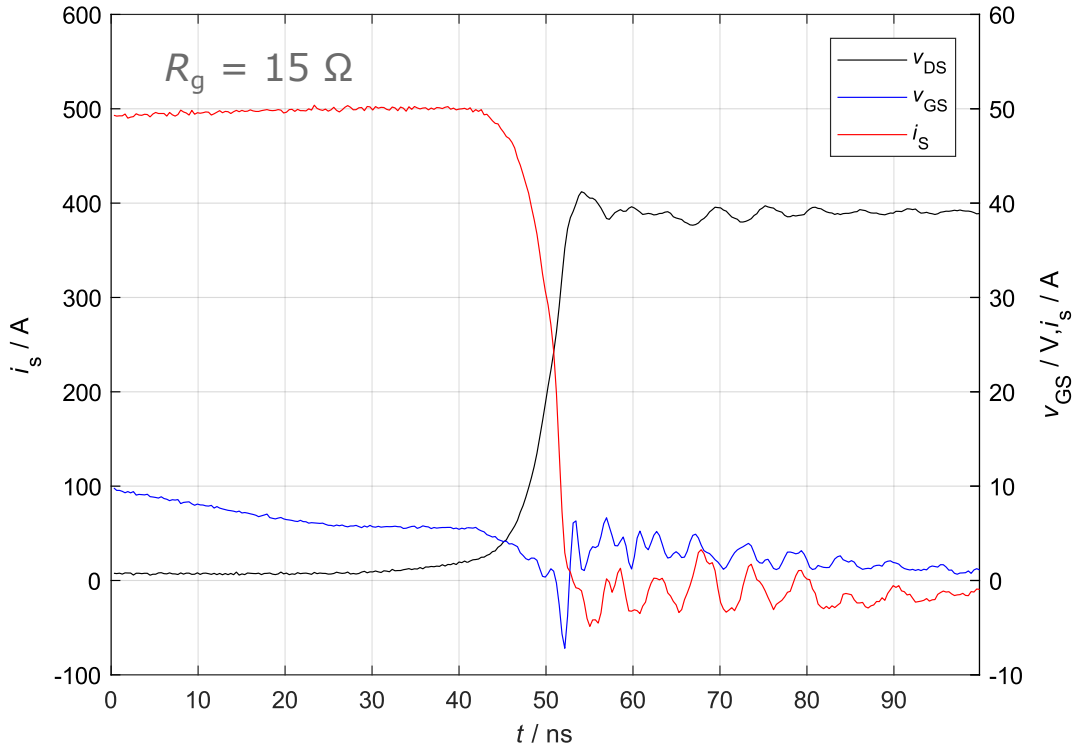
Turn-on at 50 A

E_{on}:	300 µJ
di/dt:	5.7 A/ns
dv/dt:	-69 V/ns

Double pulse results



Half-bridge with current measurement

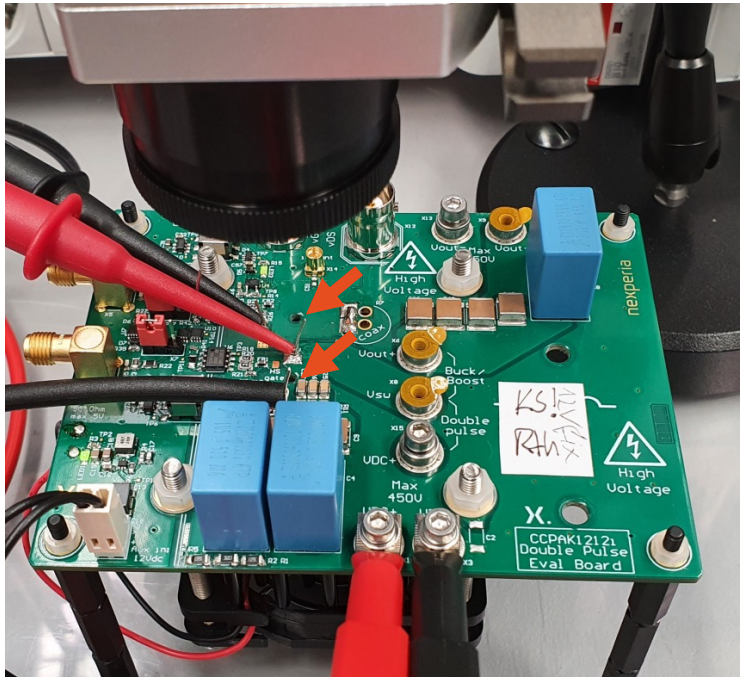


Turn-off at 50 A

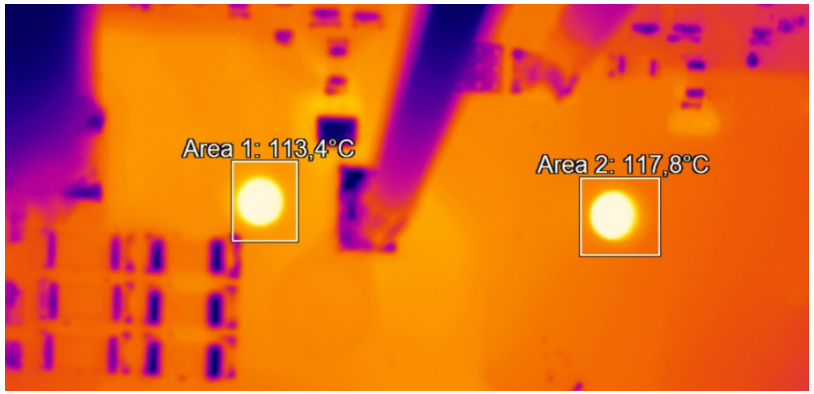
E_{off}: 35 µJ
di/dt: -7.3 A/ns
dv/dt: 45 V/ns

Thermal evaluation

- For evaluation of R_{th}, the shoot-through protection on the PCB can be deactivated
- DC current through the devices enables easy determination of device losses
- Temperature of the packages can be measured through holes in the PCB



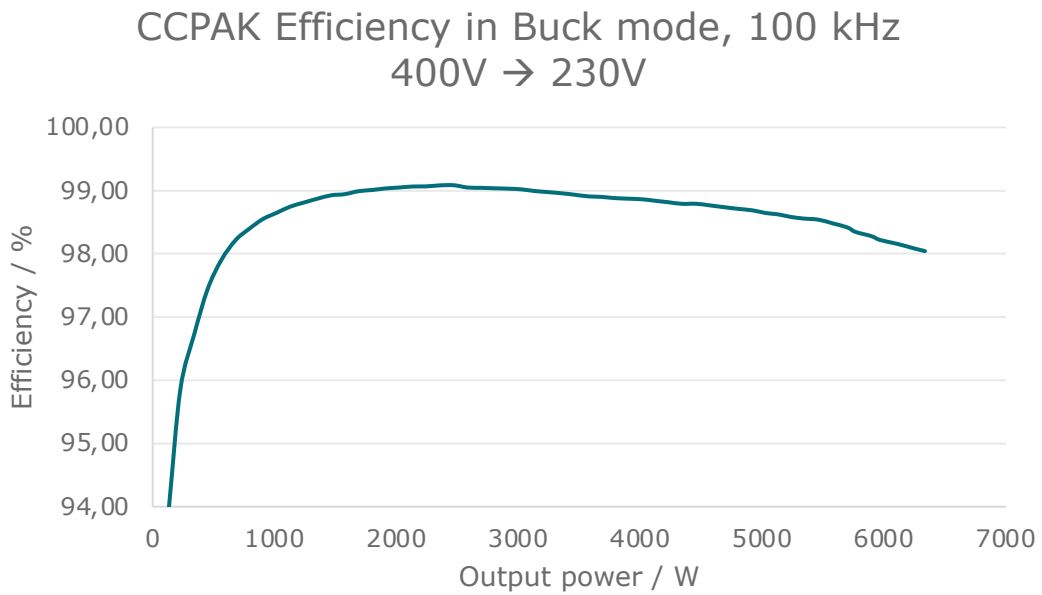
- <u>Standard setup of the Eval. board:</u>
  - Pin-Fin Heatsink & AlN ceramic insulation
  - $R_{th,ja} = \Delta T / P_{device} \approx 3$ K/W

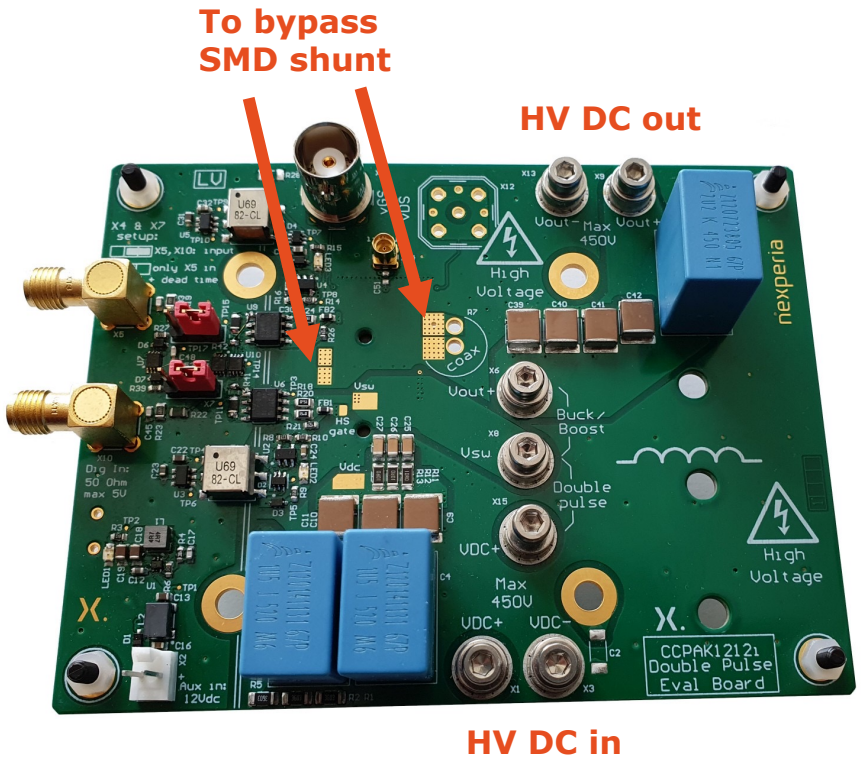


Thermal image

Continuous operation

- For continuous operation, the SMD shunt has to be bypassed using solder bridges
- Efficiency at 100 kHz with MPP toroid inductor up to 99%





Further information

Please visit Nexperia.com/GaN-FETs

Nexperia GaN FETs - Performance, efficiency, reliability brochure

MOSFET and GaN FET Application Handbook

Focus package: CCPAK

GaN FETs

Efficient and effective high-power FETs

Details | Parametric search | Packages | Documentation | Datasheets | Technology Hub | Cross reference

Datasheets (6)

Type	Title	Date	Download
Data sheet	650 V, 33 mOhm Gallium Nitride (GaN) FET in a CCPAK1212 package	2021-04-19	GAN039-650NBBA
Data sheet	650 V, 33 mOhm Gallium Nitride (GaN) FET in a CCPAK1212i package	2021-04-19	GAN039-650NTBA
Data sheet	650 V, 33 mOhm Gallium Nitride (GaN) FET in a CCPAK1212i package	2021-04-19	GAN039-650NTB
Data sheet	650 V, 33 mOhm Gallium Nitride (GaN) FET in a CCPAK1212 package	2021-04-19	GAN039-650NBB
Data sheet	650 V, 35 mΩ Gallium Nitride (GaN) FET in a TO-247 package	2021-01-12	GAN041-650WSB
Data sheet	650 V, 50 mOhm Gallium Nitride (GaN) FET	2020-07-31	GAN063-650WSA

Application notes & white papers

Understanding Power GaN FET data sheet parameters

AN90005

Circuit Design and PCB Layout Recommendations for GaN FET Half Bridges

AN90006

GaN FET technology and the robustness needed for AEC-Q101 qualification

White paper

Lastest news and blogs

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